



# **8 Channel Fiber Optically Linked Data Acquisition System for Booster Modulators**

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## **Abstract**

In order to give an immediate boost to the beam energy between the Linac and the Main Injector, the Radio Frequency (RF) Booster accelerator needs to maintain high extraction energy. The RF amplifier provides this energy but the power supply to the RF amplifier comes from a 30 kV anode Modulator. This anode modulator has been in use for over 30 years and it is desired to replace it with a new one, which is easier to maintain. The design for 30 kV anode modulator used in the Main Injector was chosen as a replacement. However, this modulator design requires a data acquisition system, since by design its high voltage deck is located at the back of the modulator. The data acquisition is made up of a transmitter and a receiver, with a fiber optic cable between them. This combination is then used for back-to-back configuration to provide noise free transmission of digital signals across the fiber optic cable.

Analog signals from the high voltage deck are applied as inputs to the transmitter. From here the signals are converted to digital signals and completely encoded before being sent over fiber optic cable. The arriving signals are then decoded and converted back to analog signals before being directed to the meter panel located at the front.

# Introduction

The Booster beam is accelerated by application of RF (Radio Frequency) energy. This energy is delivered to the beam as it passes through the cavity resonators (simply referred to as “cavities”) located in the Booster accelerator where a 100kW power amplifier drives each one. The power supply to these cavities comes from a 30kV anode modulator. Additionally, manipulations of the beam for various experiments at Fermilab require either decreasing or increasing the RF level. These functions are carried out with the 30 kV anode modulator. In order to keep up with expected energy level in the Booster accelerator, and also to be able to carry out various manipulations of the beam, the modulator needs to operate reliably at all times.

Currently, the Booster 30 kV anode modulators have been in use for nearly 30 years, and it is getting increasingly difficult and expensive to obtain parts for maintenance. It is therefore desirable to replace the modulator with a new one that is easy to maintain.

Various modulator designs were considered. Among other factors considered were cost and availability of parts for maintenance. A brand new design will have to go through all stages of design, approval and manufacturing – an impracticable option. After a series of deliberations, it was therefore decided that a closer look should be taken at all 30 kV Anode Modulators already in use. Eventually, the main injector 30 kV anode modulator was selected for use as a replacement to the current one.

This new modulator has an inherent problem. The problem results from the fact that when this modulator is installed, the capability to read the voltage and current meters on the High Voltage Deck is lost. This is because, unlike the present modulator, the high voltage deck is located at the back and there is no access space left when the modulator is fully positioned. Since the reading of the current and voltage meters are required for safe and efficient operation of the RF accelerator, there is the need to design a data acquisition system, which can transmit noise free signals from the back to the front of the modulator.

Hence this paper will describe two goals:

1. Design a data acquisition system.
2. If successful, the design will be used for all booster modulators.

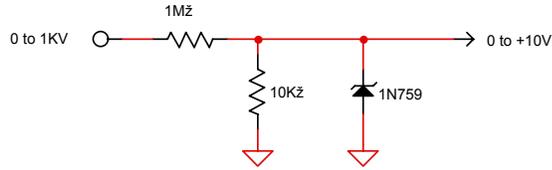
The new design is comprised of a transmitter, which is mounted on the high voltage deck, and a receiver situated at the front. In all, an eight-channel data acquisition system is sufficient to measure all the necessary readings from the high voltage deck. These values include:

1. Y567 Screen Voltage
2. Y567 Screen Current
3. Y567 Grid Voltage
4. -750V Power Supply
5. Y567 Filament Current
6. Modulator Output Current
7. 4CW800F Cathode Current
8. Overcurrent Trip Status

These required readings involve high values; hence some resistive networks were incorporated to scale the high voltage measurement to +/- 10V. This is to provide acceptable input in the analog-to-digital converter (considered to be the brain of the transmitter). This network included the application of a voltage divider as shown below.

**Figure 1. H.V. Deck Interface Signals to 8ch F.O. Transmitter**

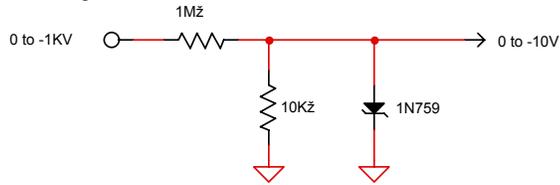
**a. Y567 Screen Voltage**



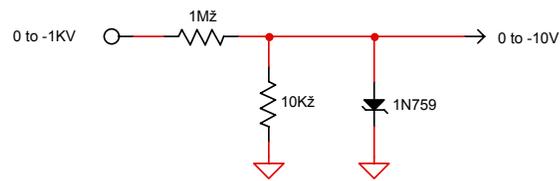
**b. Y567 Screen Current**

The screen current will be interfaced via the Isolation Amp Card EB-181091

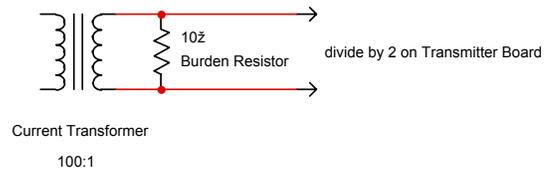
**c. Y567 Grid Voltage**



**d. -750V Power Supply**



**e. Y567 Filament Current**



**f. Modulator Output Current**

From Overcurrent Trip Board, pin #13, straight into Transmitter Board

**g. 4CW800F Cathode Current**

The 4CW800F Cathode Current will be interfaced via the Isolation Amp Card, EB-181091  
1A = 1V

**h. Overcurrent Trip**

TTL level from overcurrent trip board, pin#10, straight in, no divider

30kV Anode modulator currently being used.  
The high voltage meter panel is located at the front.



Picture 1. The current 30kV Anode Modulator used in the RF booster system. The picture shows the high voltage deck readings located on the front meter panel.

The new 30kV Anode modulator.  
The high voltage meter panel is located at the back.



Picture 2. The new main injector 30kV Anode Modulator. The high voltage deck readings are located at the back. If there is not enough space at the back these the meter panel cannot be read hence the need for the data acquisition system.

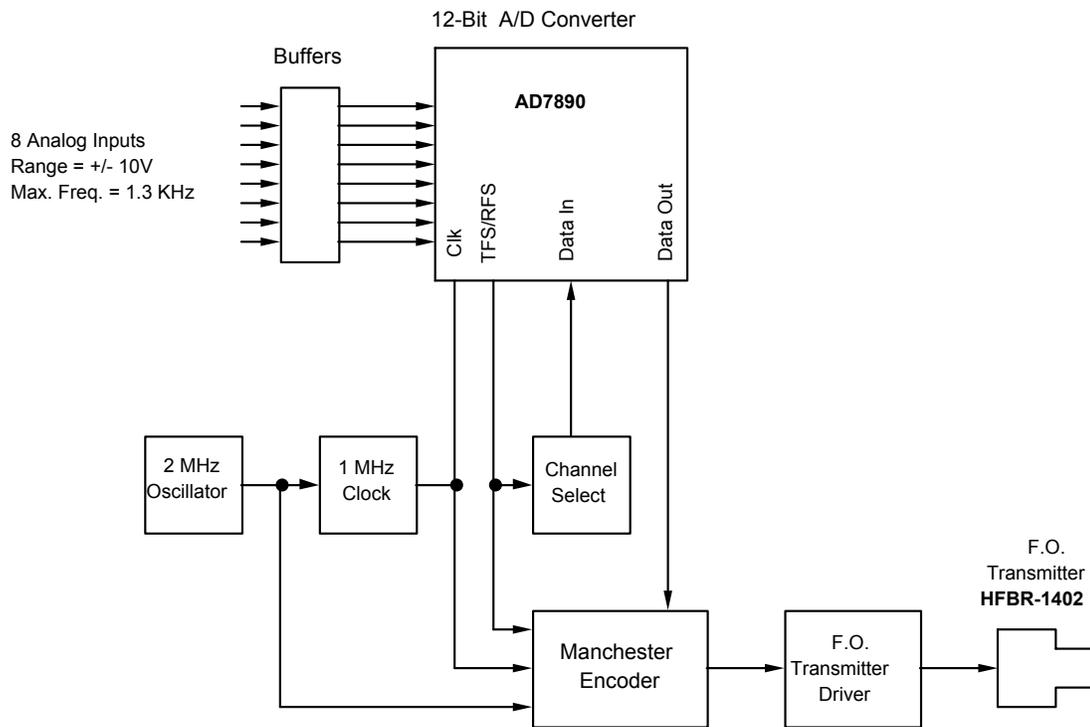


Figure 2 . 8 Channel Fiber Optically Linked Data Acquisition System - Transmitter

## Theory of Operation

The 8-channel data acquisition system will consist of a transmitter and a receiver board connected by fiber optic cable. The analog signal is first converted to a digital signal by the analog-to-digital converter (AD 7890). This signal is then encoded and sent through fiber optic cable to the receiver. The digital output is a 16-bit Manchester encoded serial output. This output signal is then transmitted through a fiber optic link as shown in figure 2 above.

The receiver board receives the encoded serial data via fiber optic cable. Next, the data is decoded and converted back to an analog signal. The signal is then buffered and scaled to drive their respective meters as shown in figure 3.

### Transmitter

The transmitter is built around the AD 7890. The AD 7890 is a complete eight-channel, 12-bit data acquisition system, which accepts an analog input range of +/- 10V. The transmitter has eight basic sections:

1. Oscillator
2. Clock
3. Buffers
4. 8-channel, 12-bit Data acquisition System
5. Channel Selector
6. Manchester Encoder

7. Fiber Optic Transmitter Driver
8. Fiber Optic Transmitter

Oscillator. The Oscillator frequency is 2 MHz. This 2 MHz clock is used as a source of spaced pulses and it is used as a time clock for the Manchester encoder.

Clock. The clock signal frequency is 1 MHz. A J-K positive edge-triggered flip-flop is used to divide the 2 MHz signal down by 2. Since the 2MHz signal is fed into the CLK, the output will change states every half cycle of the input signal producing a 1 MHz signal.

Buffers. Eight buffers are inserted into the AD 7890, one for each channel. They are configured as voltage followers and provide the necessary drive to the inputs of the AD 7890. They made up of sample and hold amplifiers and positioned between the transmitter and the high voltage divider. This voltage divider is made of two resistors and a diode, and is used to scale down the high voltage signals.

Channel Selector. This consists of a 4-bit binary counter and 8-bit shift register. The binary counter is designed so that channels 1 to 8 are read sequentially and continuously. It counts from 0000 to 1111. Only the 3 least significant bits are used to load into the shift register. The shift register converts parallel data to serial data, which is sent to Data In on the AD 7890.

8-channel, 12-bit Data Acquisition system. The AD 7890 is a fast 12-bit, single supply serial data acquisition system with 5.9  $\mu$ s conversion time. It has eight single-ended analog input channels, which are used for the 8-channels. It comes with signal scaling multiplexer, track and hold reference, and a serial logic function on a single clip. It accepts +/- 10V signals. The equipment serves as the brain of the transmitter by providing access to the multiplexer output. This affords one initializing filter to be used on the output of the multiplexer, to provide the initialing function for all eight channels. It also has various input/output outlets, notably TFS/RFS, CLK, Data in and Data Out which are used to complete the conversion process.

Manchester Encoder. This is used to provide clock and data information simultaneously via a single connection. The rising/falling edge in the center of the data bit indicates either a logic "1" or alternatively a logic "0". This equipment is used with the 2 MHz clock for encoding the digital signal before being transmitted down fiber optic cable. The coding process involves mixing the clock with serial data. This creates a mid-bit transition every half cycle where all 1's are changed 1 0 and 0's to 0 1.

Fiber Optic Transmitter Driver. This equipment provides full duplex, asynchronous communication over the fiber optic cable. It has the benefit of immunity from EMI/RFI interference and provides secure data transmissions.

Fiber Optic Transmitter. This is a self-contained fiber optic data transmitter. It serves as a source of signal coupled into the fiber optic cable. Additionally, it

modulates the encoded signal so as to reproduce the binary signal it receives from the Manchester encoder. By so doing it converts the encoded signal from the Manchester encoder into a fiber optics signal for transmission via a single mode fiber optic cable.

## **Receiver**

The receiver is built around the digital-to-analog converter (ADDAC80). The ADDAC80 is a complete 12-bit digital to analog converter, which accepts a digital input range of 0V to +5.0V.

The receiver has seven basic sections to it:

1. Fiber Optic receiver
2. Manchester Decoder
3. Digital to Analog Converter (ADDAC80)
4. Channel Selector
5. Buffers
6. Burndy Connector

Fiber Optic receiver. The fiber optic receiver is mainly used to sense the signal coming from the fiber optic cable. It also demodulates the signal to determine the binary data it represents. Once the incoming data is identified, the receiver then transmits the data to the Manchester decoder.

Manchester Decoder. The Manchester decoder accepts Manchester encoded data at a given bit rate and output the recovered clock and the original data. This design assumes a decode clock at nominally eight times the incoming data rate. Hence the circuit tolerates substantial frequency errors between encoder and the decoder. The recovered clock and data signals are presented on a serial to parallel converter with the data signal inverted.

Digital to Analog Converter. The ADDAC80 is a 12-bit, high-speed digital-to-analog converter with both a high stability voltage reference and an output amplifier combined on a single monolithic chip, with analog output of +/- 10V. This allows it to accept complementary digital input code in binary format. It converts the digital signal to analog signals and transmits the output to the buffers. It is also compensated to settle within 1/2 least significant bits for a 10V full-scale transition in 2.0 us.

Channel Selector. This is made of a binary counter and a shift register. The binary counter is made of two flip-flops connected together and designed so that channels 1 to 8 are read sequentially and continuously. It only gives 3-bit address channels to be read. The shift register is used to convert serial data to parallel.

Buffers. Eight different buffers are used. They serve as a conduit between the receiver and the meters. They are simply used to pass data and current to the meters.

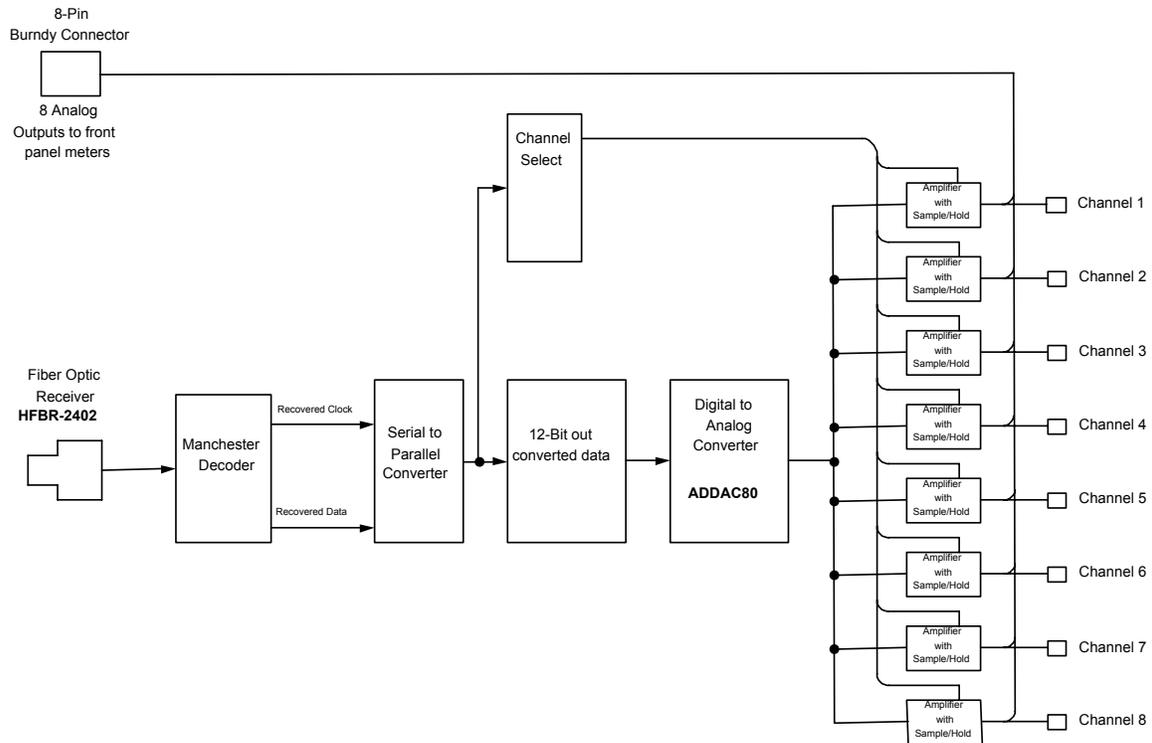


Figure 3 . 8 Channel Fiber Optically Linked Data Acquisition System - Receiver

Burndy Connector. These accept analog signal from of the sample and hold amplifiers to the front panel meters.

### **Materials needed**

1. Buffers
2. 12-bit AD790 AND 12-bit ADDAC80
3. Clock 2MHz and 1MHz
4. Manchester encoder/decoder
5. Channel selector
6. Track/hold amplifiers
7. Transmitter and Receiver boards
8. Fiber optic cable

## Experimental Details

The high voltage analog signal is first scaled to +/-10V, by connecting a diode and two resistors in parallel with a common 1M $\Omega$  resistor. This combination also serves as a buffer between the high voltage deck and a transmitter. The analog signal from the deck interface is then sent to the analog-to-digital converter via the buffers. On reaching the analog-to-digital converter, the signal is scaled to +2.5V down to the multiplexer. Since the AD7890 will operate in the external clocking mode, the process of reading data in the multiplexer part of the AD7890 is done with the help of a 1 MHz clock. This clock is also used to synchronize the transmitter and the receiver to ensure both operate on the same time clock.

The analog-to-digital converter serves as the brain of the transmitter. It sets the transmitter working with its TFS/RFS unit. The Transmit Frame Synchronization Pulse and Receive Frame Synchronization (TFS/RFS), which provides a strobe, or framing pulse internally generates an active low output. This comes in the form of a rectangular pulse with the higher level corresponding to 1 and the lower line corresponding to 0. This pulse is also a clock, which triggers the binary counter into action. The binary counter is designed in such a way that it enables reading of the 8 channels sequentially and continuously. It starts by giving 3-bit address channels to be read. The first bit counts one and corresponds to the first channel. This action then loads the 3 bits to the shift register where an internal conversion takes place resulting into 8-bit parallel data.

In the shift register, an 8-bit parallel is converted to serial data. Once the serial data status is achieved only the 5 most significant bits are read as input back to the AD 7890.

The conversion of the analog signal to digital takes place with the help of a clock input (TTL compatible clock) and an edge-triggered logic input (software). A high to low transition on this input puts the track and hold into hold and initiates conversion when the internal pulse has timed out. At the end of the conversion, TFS/RFS goes low and the serial clock and the data out becomes active. The data out contains 16 bits of data with one leading zero preceding the three address bits of the control register and the 12 bits of conversion data.

The data out is then sent to the Manchester encoder where it is encoded with the help of a 2 MHz clock. The coding process involves mixing the clock with serial data where the rising/falling edge in the center of the data bit indicates either a logic "1" or alternatively a logic "0". This creates a mid-bit transition every half cycle and all 0 1s are changed to 1 0s and vice versa. The final output from here is a complete encoded signal ready to be sent via fiber optic cable to the receiver. Figure 4 shows the final outputs of the various parts of the transmitter.

Fiber optic cable is used as the means of sending the signal because of its numerous advantages. Firstly, the signal is transmitted further without needing to be "refreshed" or strengthened. Secondly, this cable has greater resistance to electromagnetic noise such as motors or other nearby cables. Thirdly, fiber optic networks operate at high speed and optic cables costs much less to maintain.

The encoded data is delivered to the receiver through a fiber optic cable. The signal initially goes to the Manchester decoder where it is decoded. On completion of decoding the data is separated into recovered clock and serial data.

The serial data goes into the serial to shift register where it is converted to 16-bit parallel data. The shift register has a D-type flip-flop attached to it. This serves as a buffered clock. The clock triggering occurs when the shift register is fully loaded.

The shift register also has a binary counter. This is turned on during the recovery of the clock data and the experimental data from the decoded signal. It becomes effective as soon as the shift register is fully loaded.

The 16-bit signal is transmitted to the D-type flip-flop. Here the leading zero is ignored and the remaining bit separated into two parts. The three-address bit is passed onto a data transmission system. During this time the 12-bit data is also transmitted to the digital-to-analog converter. The output from the DAC is an eight channel analog signal.

The data transmission system uses the 3-address bits to determine which channel is selected first. From here the signal is passed on to the respective deck meters.

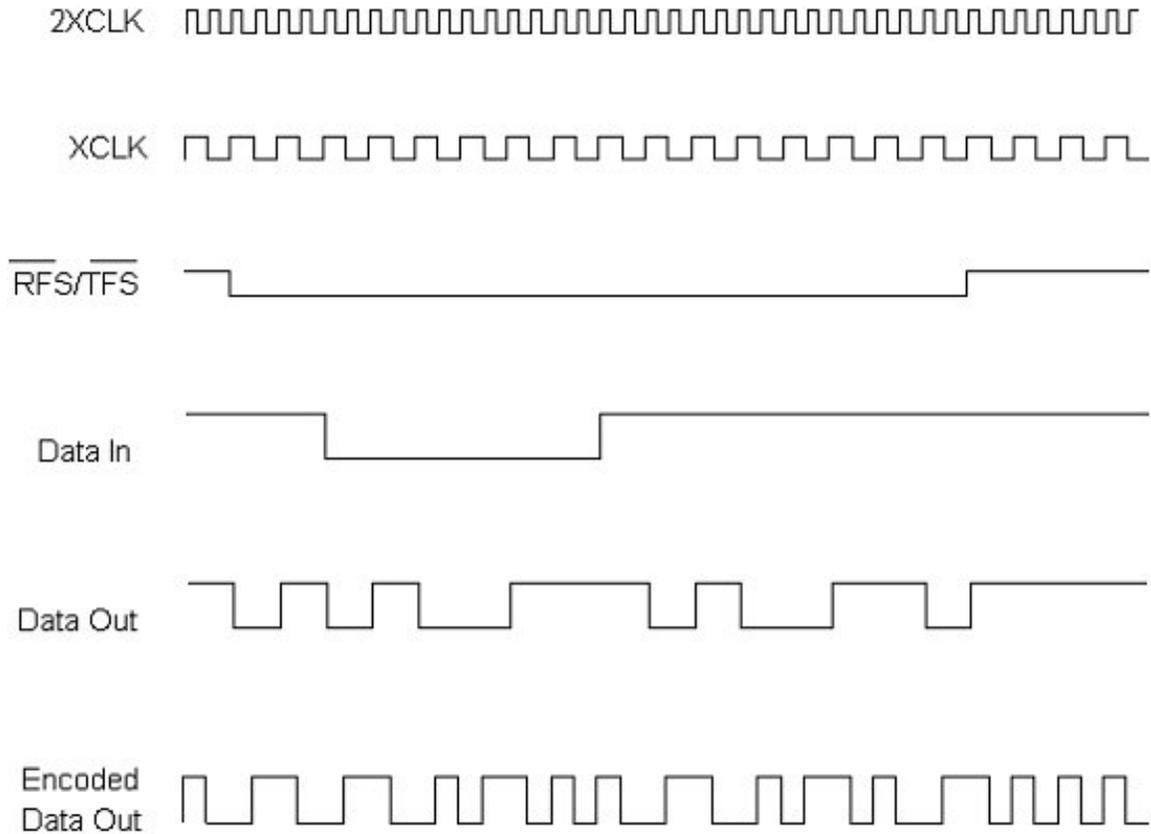


Figure 4. The timing diagrams of the various output of the transmitter.

Figure 4 above shows the timing diagram of the expected outputs of the transmitter. The first two diagrams show the expected output of the 1 MHz and 2 MHz clocks. The RFS/TFS also shows signal expected when the pulse goes low. During this time, 16 square pulses will be transmitted before the signal goes up again and the data in from the shift register will be as shown against Data In. The serial data to the AD 7890 will then be converted to a digital signal. It is expected that the data from the analog to digital converter will be in the form as shown against Data Out. This data will then be encoded before being transmitted over the fiber optic cable. It is expected that the encoded signal be in the form shown against Encoded Signal Out ready to be sent to the fiber optic transmitter.

## Results and Discussion

Figures 5 and 6 below show the various outputs from the first phase of the transmitter operation. The first image is the output of the 2 MHz clock. Compared to the timing diagram expected, the pulses are almost identical. It shows that 32 pulses are transmitted when the RFS/TFS goes low as expected.

The second image is the output of the 1 MHz clock. As predicted, it shows 16 pulses are transmitted anytime the RFS/TFS goes low. The sixteen pulses are responsible for the 16-bits that are expected that are transmitted.

The third picture is the output of the RFS/TFS. The high portion indicates a 1 and the low portion 0. As expected the pulse stays low for the transmission of the number of bits required. This output confirms exactly what is expected.

The picture labeled 4 is the input to the AD 7890. It represents the eight bit serial data, which goes to the analog converter as Data In.

Overall, the data displays a consistent agreement with the theoretical prediction of the timing diagram as outlined earlier. There are certain aspects of the timing diagram that are worth clarifying. The presented result represents all the output of the transmitter which are used. As suggested earlier, the 2 MHz clock was able to transmit 32 pulses when the TFS/RFS goes low. During this time the 1 MHz clock also transmits 16 pulses. The 1 MHz clock timing diagram shows more success than the 2 MHz clock.

A clear examination of the Data In shows much success. The timing diagram shows the leading zero and the five most significant bits being returned to the analog-to-digital converter. Even though it was difficult to get straight edges, despite their shape, they do present the needed bits.

In regards to the diagram depicting data coming out of the analog-to-digital converter, it clearly shows the 16-bit digital data. The pulse shapes were marked clearly with straight edges. This is a much more successful result compared to the previous trails.

The encoded signal came out as expected. This output depends on the value of Data Out; hence its timing diagram is a fair representation. The mid-point transition came out clearly, even though further improvements on the transmitter design could have helped produce smoother pulse edges.

Figure 5. 1 and 2 MHz clock with TFS/RFS and Data In.

1---→ 2 MHz.

2. ---→ Data In

3----→ TFS/RFS.

4---→ 1MHz

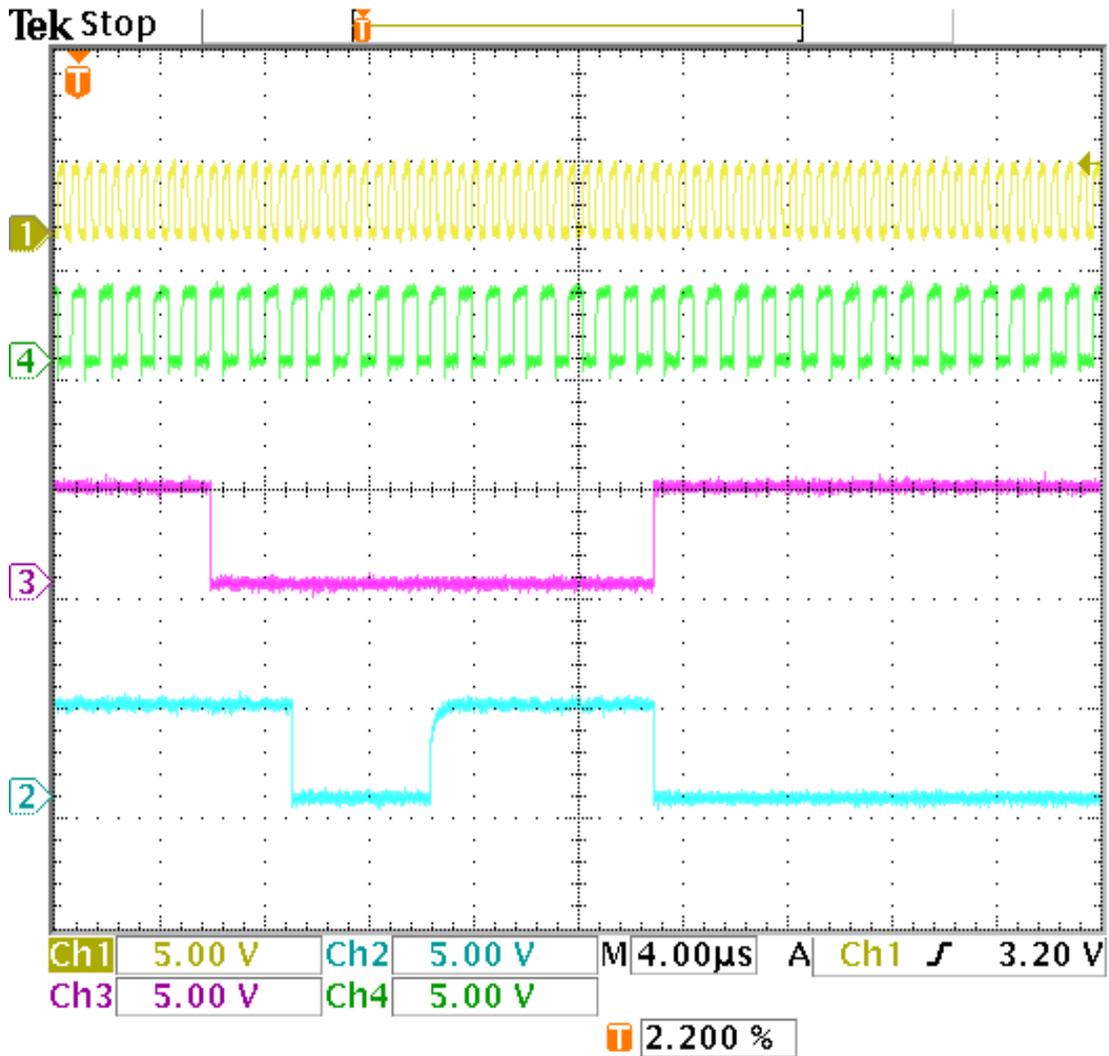


Figure 6. Outputs various component of the transmitter.

1-----> RFS/TFS

2. -----> Data In.

3. -----> Data Out

4-----> Encoded signal ready to over fiber optic cable.

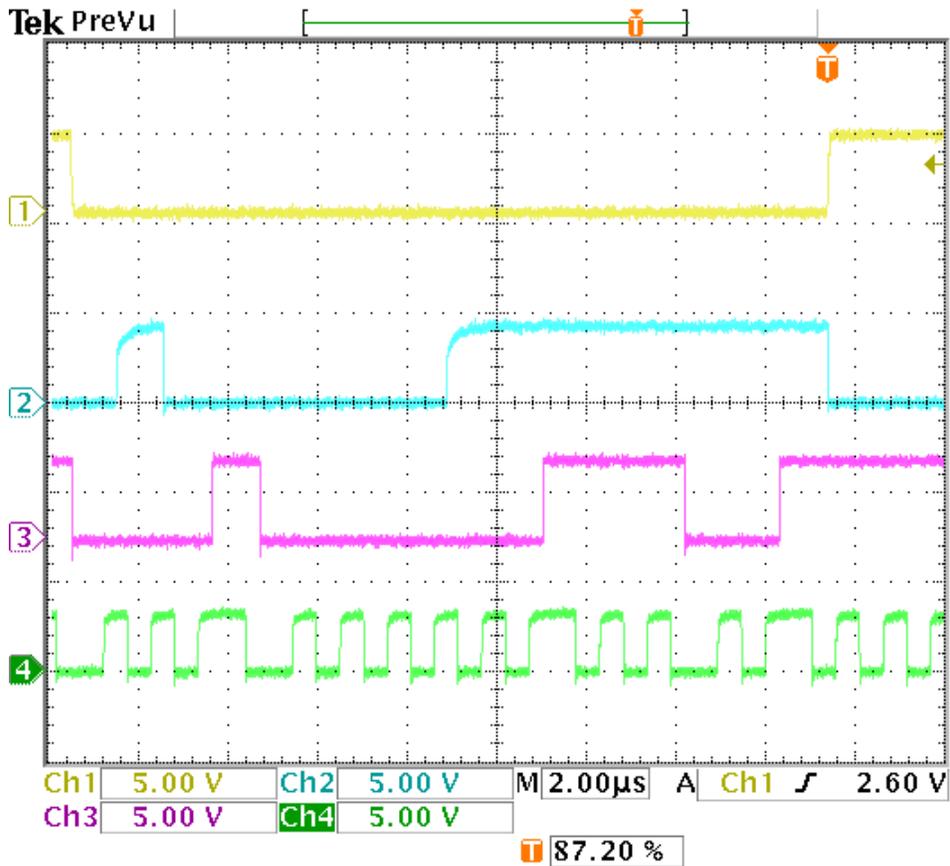
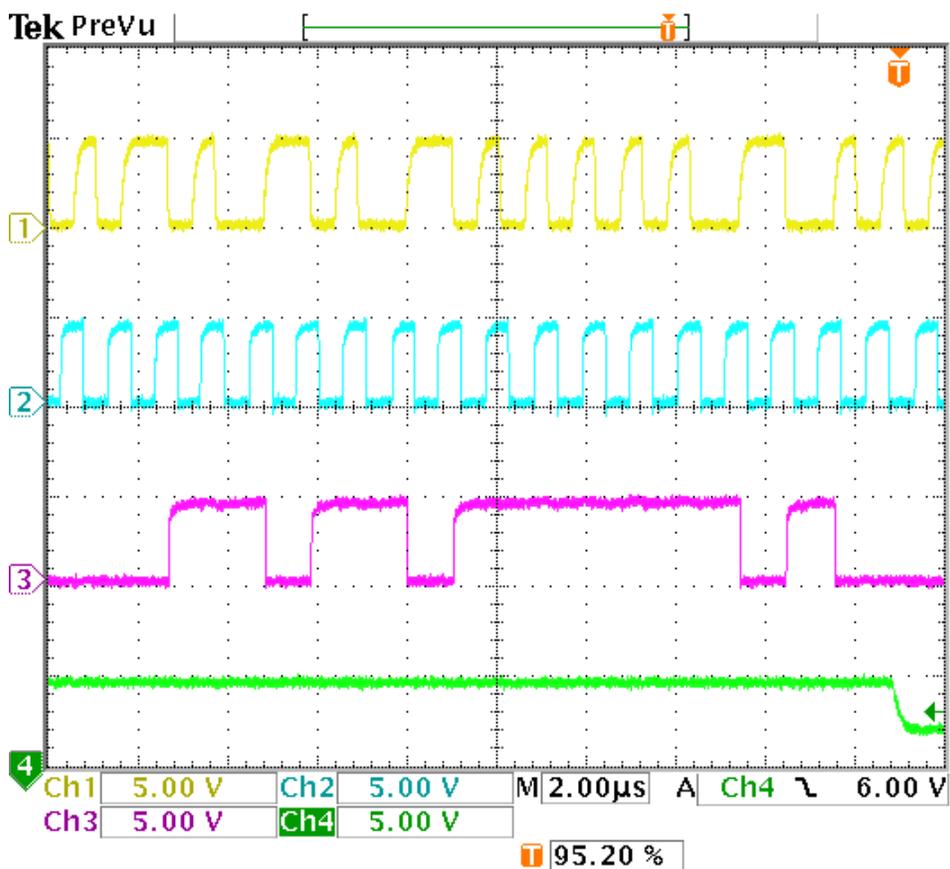


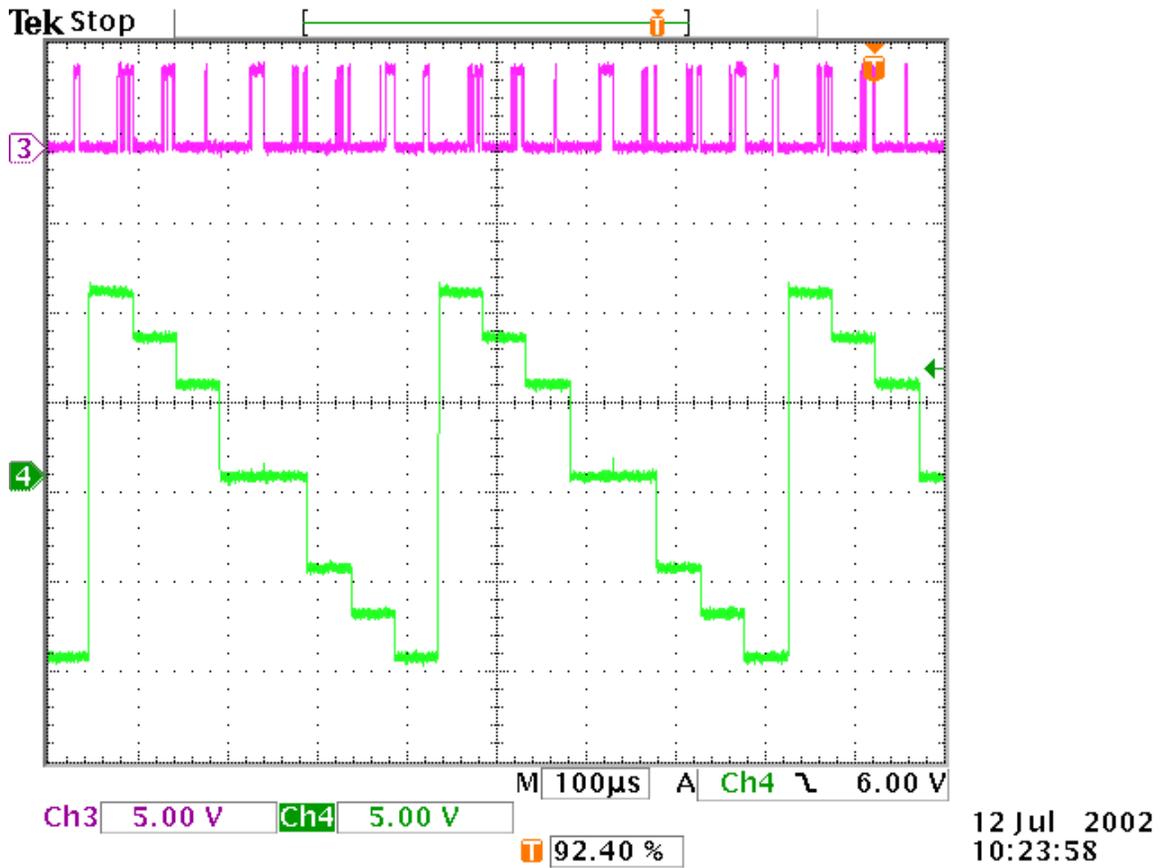
Figure 7. Outputs of the receiver.

- 1-----→ Encoded signal from the decoder
- 2-----→ Recovered 1 MHz clock
- 3-----→ Decoded signal
- 4-----→ Analog signal ready for deck meters



12 Jul 2002  
10:22:31

Figure 8. The experimental data coming from the receiver.  
3----→ Decoded signal  
4----→ Final 8-channel analog ready for deck meters



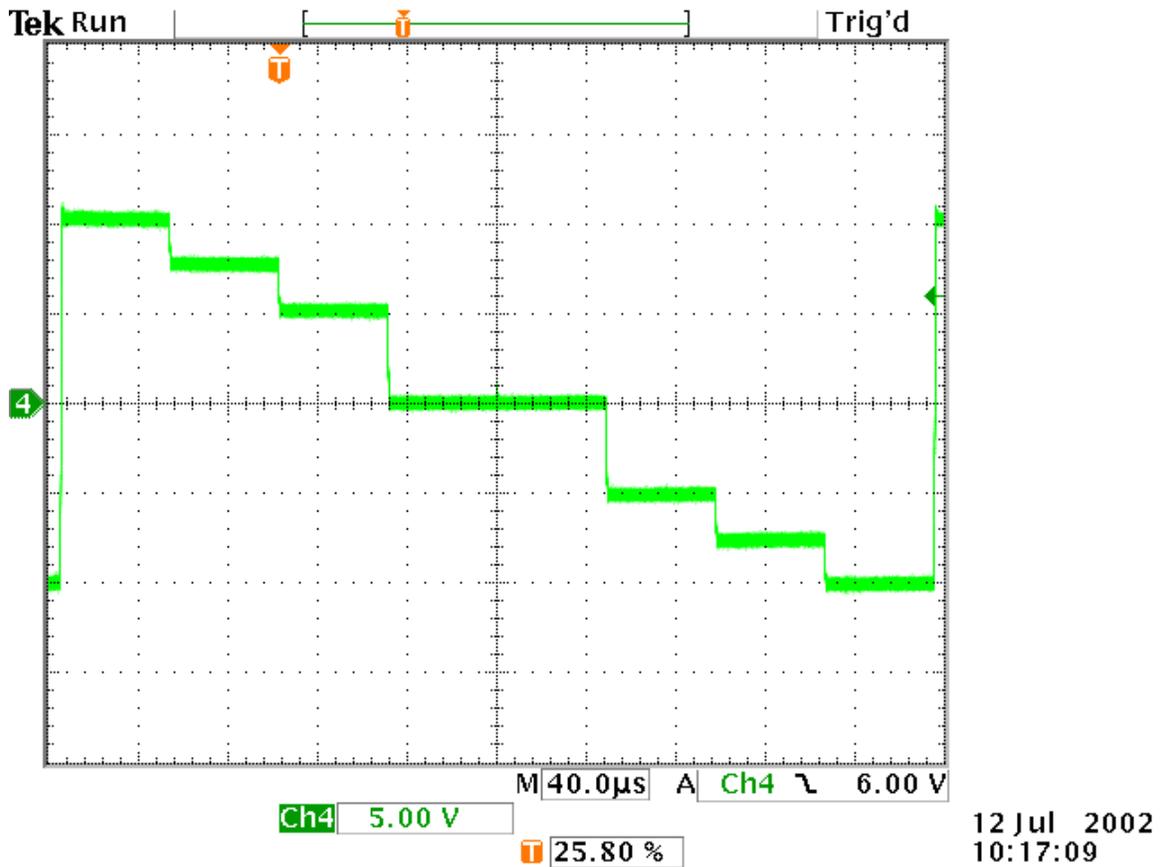


Figure 9. A clearer view of the output of the 8 channels.

Figures 7, 8 and 9 show some of the experimental timing diagram from the receiver. Overall, the diagrams display a general agreement with the theoretical predictions. In matching the encoded signal with the encoded signal leaving the transmitter, there is less success. The pulse shapes did not come out very clear even though it shows a fairly accurate representation of the data out.

Much success is achieved for the 2 MHz recovered clock. Its timing diagram came out exactly as expected. Similar results are achieved as the recovered serial data in the receiver exactly matches what was sent out in the transmitter.

The final analog signal in Figure 9 shows exactly the desired voltages that were sent from the high voltage deck to the front. It shows the scaled down +/- 10V output of the digital-to-analog receiver.

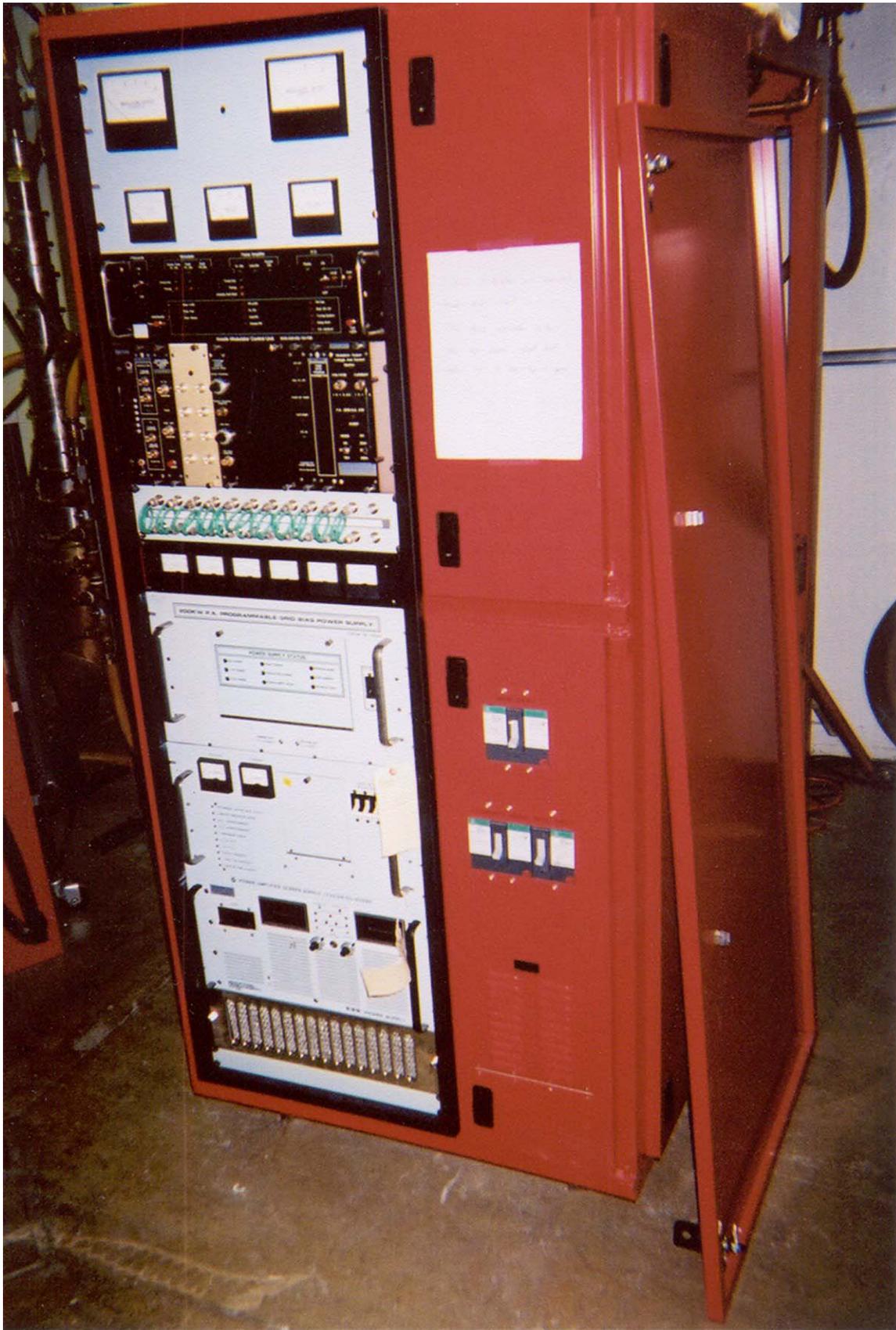
The transmitter and the receiver were then installed, the first trials carried out, and the result recorded in Table 1 below:

Table 1. High voltage readings for both the back and front meter panel of the modulator.

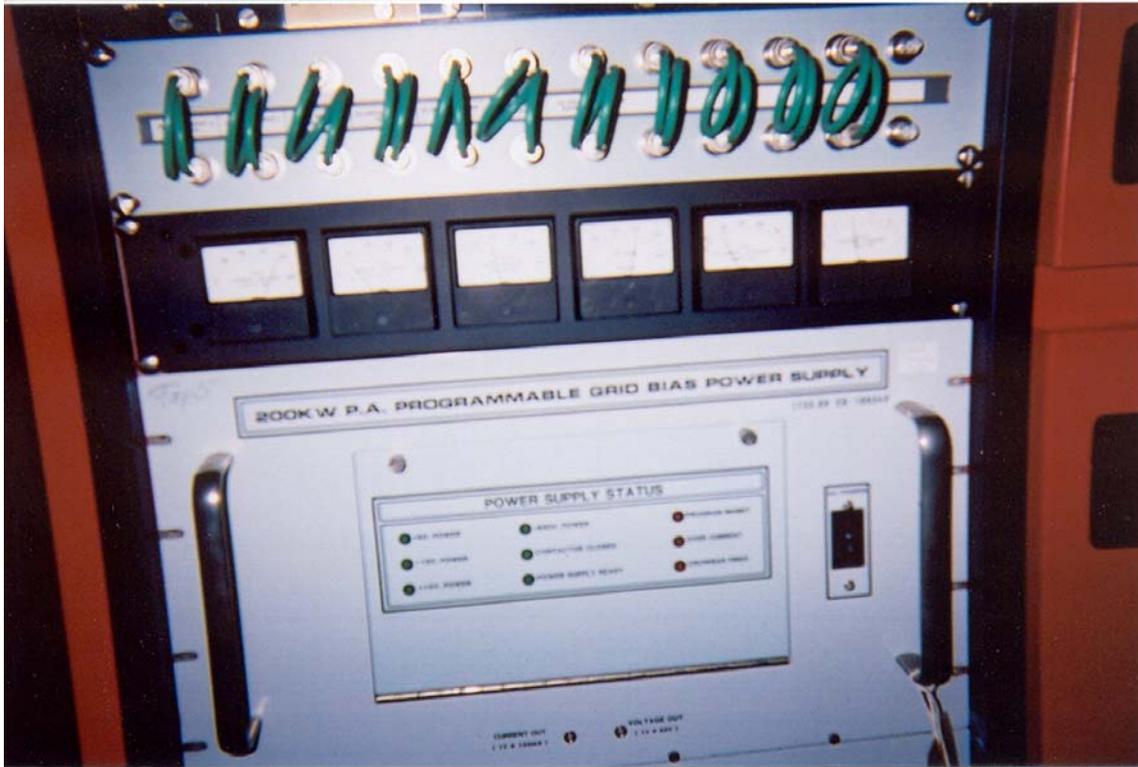
<b>High Voltage Deck</b>	<b>Back of the modulator</b>	<b>Front panel meters of the modulator</b>
Screen voltage	+800V	+750V
Screen current	80 Amps	80Amps
Grid Voltage	-400V	-380V
Cathode current	-5.8Amps	-5.9Amps
Filament current	180Amps	180Amps
Power supply	600V	X

Reasonable agreement prediction was achieved in the determining the value of screen current and filament current. Those values recorded from the back high voltage deck exactly matched those recorded from the front meter panel. Measured values of values from two other sources did not much prediction. The screen voltage recorded at the front is 50 V less; the same scenario is noticed at values from the grid voltage where its front meter panel gave  $-20$  V more reading. The same situation occurs at the cathode current where a difference of  $-0.1$  A was noticed.

These differences observed in the readings affected are largely due to the high value resistors used in the voltage divider to scale down the high voltages. Overall the results are good as shown in pictures 3 and 4 below.



Picture 3. A new look for the 30kV Anode Modulator with data acquisition system.



Picture 4. A clearer view of the front meter panel of the new modulator.

## Conclusion

In summary, the method to design a data acquisition system matches well with the theoretical predictions. This suggests the design is reliable. The interface, which was designed purposely for scaling down the high voltages to suit the respective ADC/DAC, performed superbly. Even though there exists little variations among the values obtained on the front meter panel, the effect can be minimized using low value resistors for the voltage divider.

## Acknowledgements

I want to thank my supervisor, Rene Padilla, for his insights, assistance, and his patience in guiding a physics student through this project. Even though I barely have any knowledge on electronics he did a marvelous job in helping me to grasp a firm knowledge in electronics. I also want to thank Joe Dey for resolving many of my computer issues, Mitch Adamus for guiding me through the complete installation of the

data acquisition system on the modulator, Stefanos Dris for his encouragements and support, and Bob Scala for his insights and also all the people in the RF group who made my stay here a bit more enjoyable. Finally, I want to thank Dianne Engram, Dr. Elliot McCrory, Dr. James Davenport, and the rest of the SIST committee for accepting me and for their help during this internship.

## References

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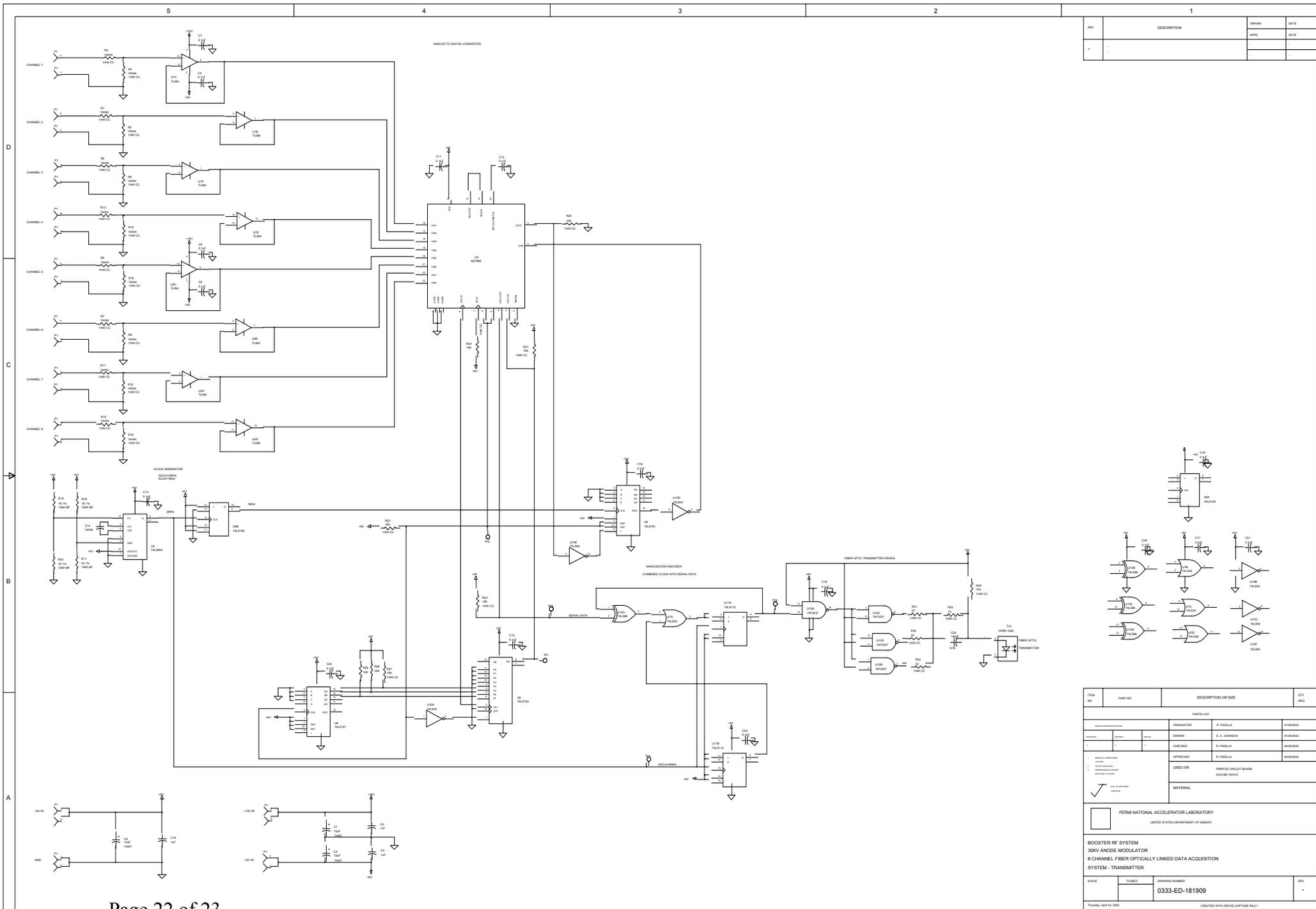
Analog Devices. (1996). 12-bit Serial Data Acquisition System. Norwood, MA. Analog Devices Inc.

Analog Devices. (2002). 12-bit D/A Converters. Norwood, MA. Analog Devices Inc.

## Appendixes

Appendix I, Schematic diagram of the transmitter.

Appendix II. Schematic diagram of the receiver.

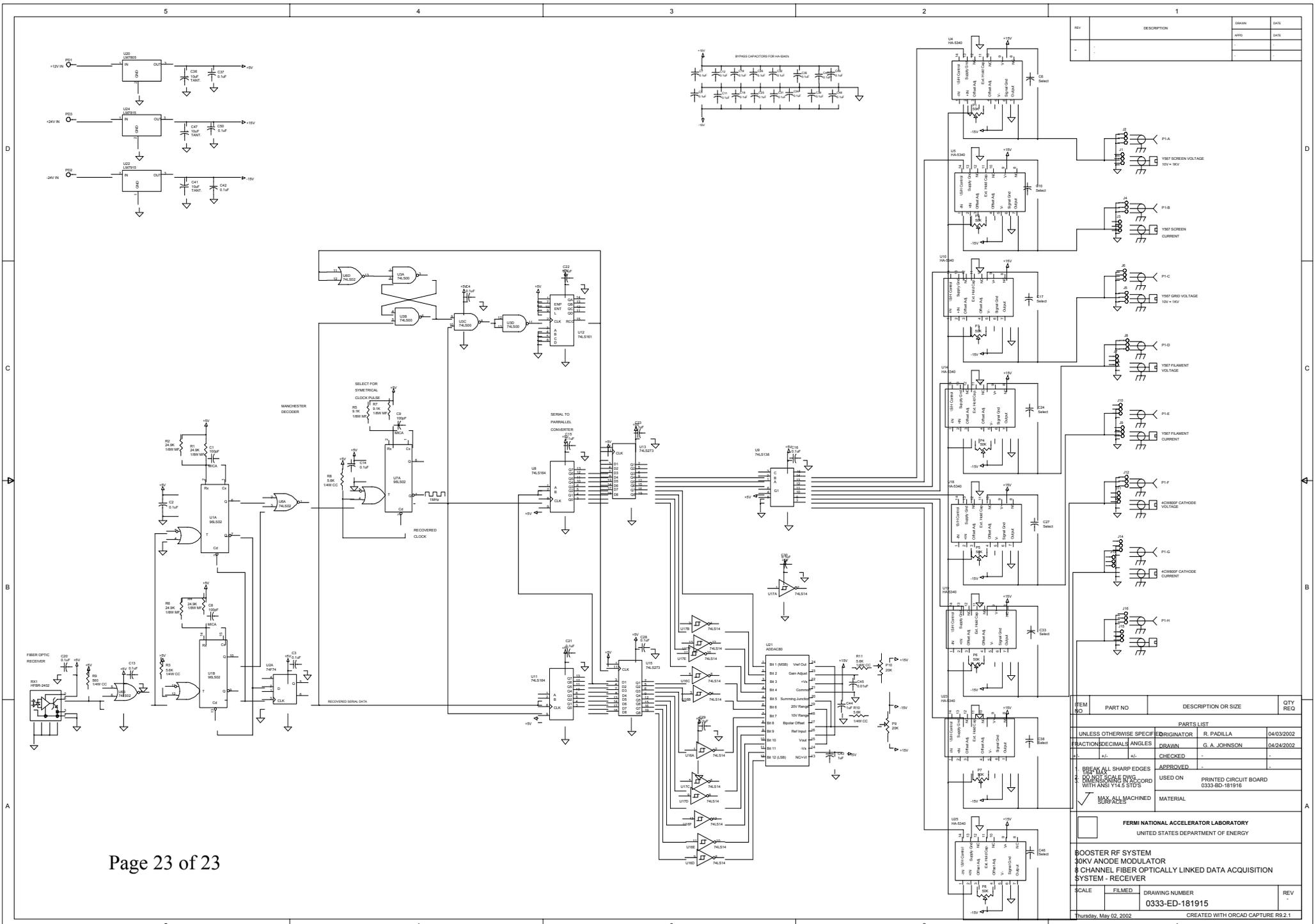


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2			

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	DESIGNED	C. A. JANSSEN	0333-0001
	CHECKED	R. PAVELLA	0333-0001
	APPROVED	R. PAVELLA	0333-0001
	USED ON	PHOTO CELL BOARD	0333-01410
	MATERIAL		

FERM NATIONAL ACCELERATOR LABORATORY  
 UNITED STATES DEPARTMENT OF ENERGY  
 BOOSTER RF SYSTEM  
 30KV ANODE MODULATOR  
 8 CHANNEL FIBER OPTICALLY LINKED DATA ACQUISITION  
 SYSTEM - TRANSMITTER  
 SCALE: DRAWING NUMBER: 0333-ED-181909 REV: -  
 Thursday, April 04, 2002 CREATED WITH ORCAD CAPTURE 8.6.1

# Appendix II, Receiver



REV	DESCRIPTION	DRAWN	DATE
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UNLESS OTHERWISE SPECIFIED				
FRACTIONS/DECIMALS/ANGLES				
DRAWN G. A. JOHNSON 04/24/2002				
CHECKED -				
APPROVED -				
USE ON PRINTED CIRCUIT BOARD 0333-BD-181916				
MATERIAL				

**FERMION NATIONAL ACCELERATOR LABORATORY**  
 UNITED STATES DEPARTMENT OF ENERGY  
**BOOSTER RF SYSTEM**  
**30KV ANODE MODULATOR**  
**8 CHANNEL FIBER OPTICALLY LINKED DATA ACQUISITION SYSTEM - RECEIVER**  
 SCALE FILMED DRAWING NUMBER  
**0333-ED-181915**  
 Rev 1  
 Thursday, May 02, 2002 CREATED WITH ORCAD CAPTURE RS 2.1