

SEQUENCER DELAY PLD

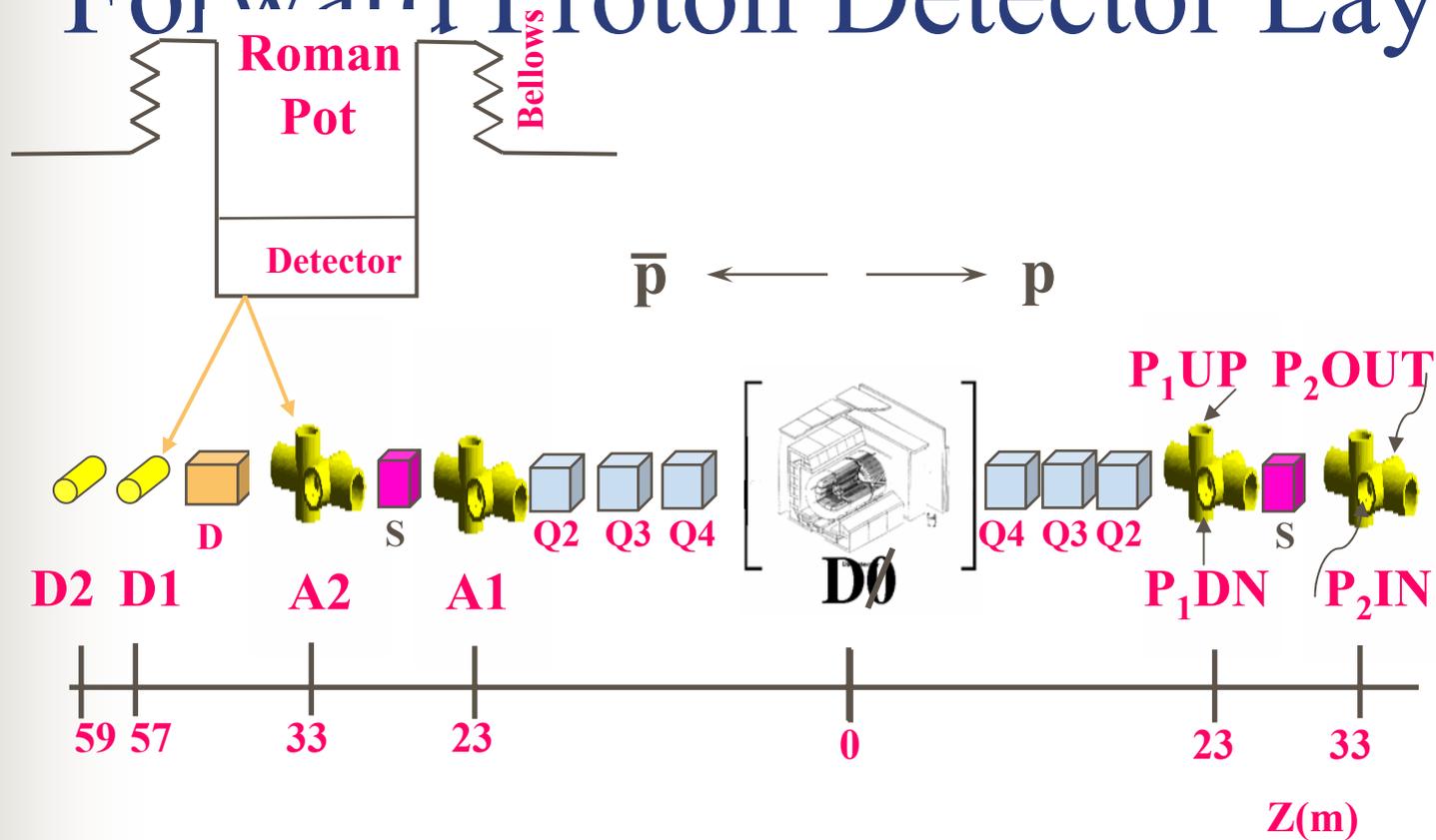


By ANTON H.C. SMITH

ELECTRICAL ENGINEERING

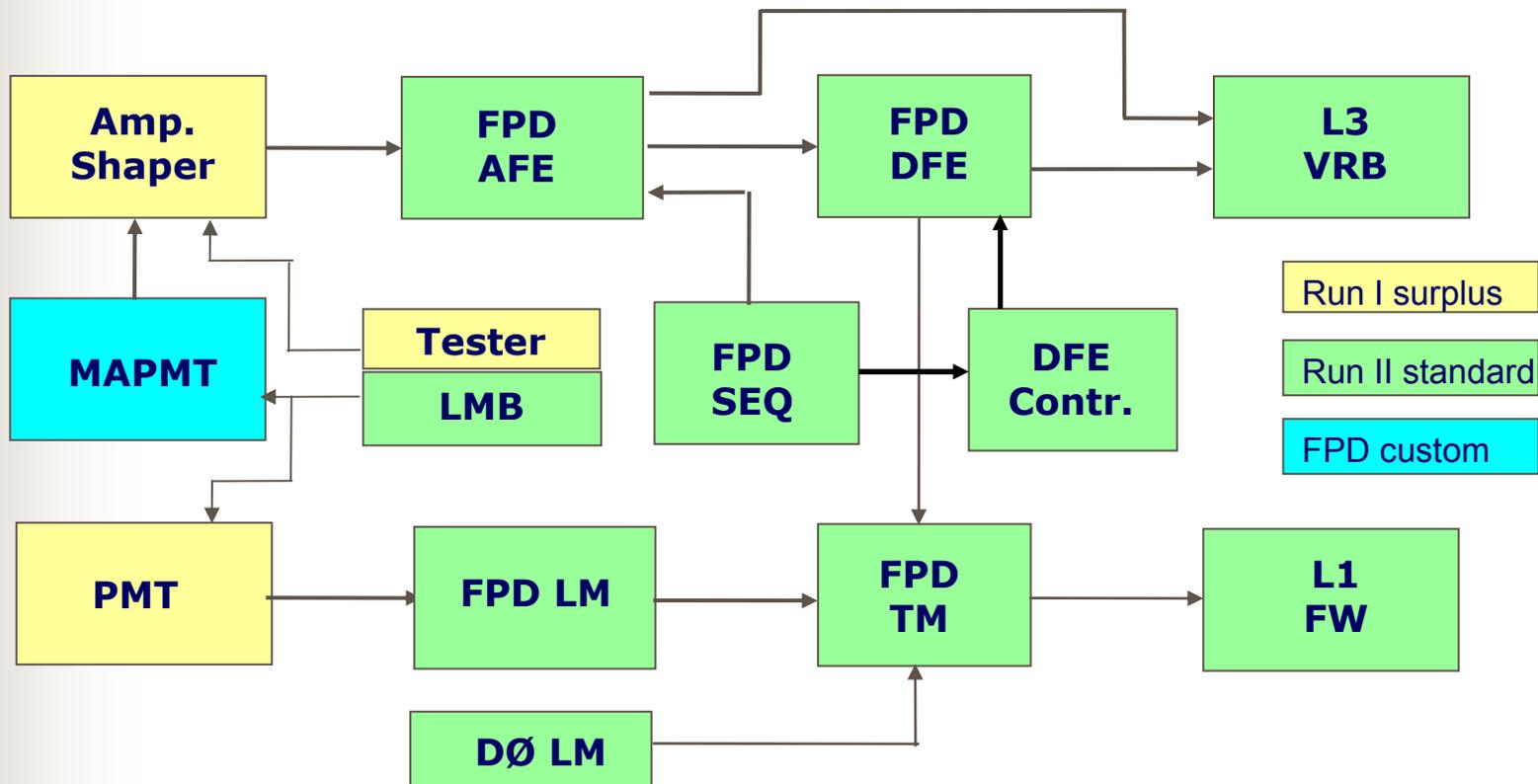
UNIVERSITY OF SOUTH CAROLINA

Forward Proton Detector Layout



- FPD is sub-detector of D0 consisting of 9 momentum spectrometers, allowing detection of scattered anti-protons and protons and determination of momentum and scattering angle
- Central systems measured in D0 Detector

FPD ELECTRONICS





Analog Front End (AFE)

- Basically the interface for the SVX chips
- Files analog information into data stream
- Digitalizes fiber information for Triggering
- Allows algorithms that looks at hit patterns of fibers in detector to select valid tracks



SEQUENCER

- Real time manipulation of the control signal to the AFE to effect data acquisition, digitization, and readout based on the NRZ/Clock signals from the Controller.

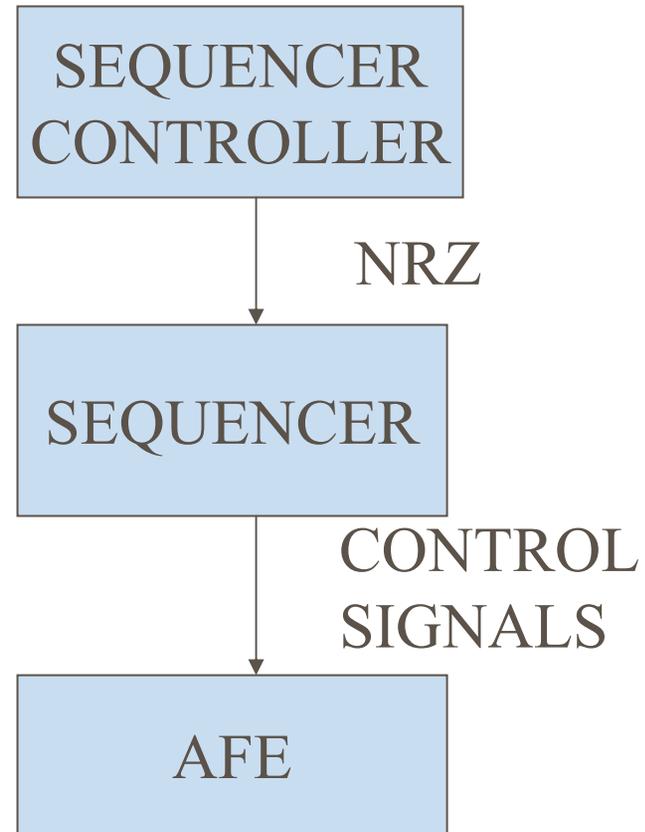


SEQUENCER CONTROLLER

- It transforms Serial Command Link (SCL) signals into pairs of Sequencer control signals (NRZ & Clock).
- These signals tell the Sequencer the proper times to reset the preamps, trigger, digitize, and read out data.

Different Methods of Implementation

- Delaying the Control Signals of the AFE
- Delaying the NRZ signal on the Sequencer
- Delaying the NRZ signal going to the sequencer from the Sequencer Controller



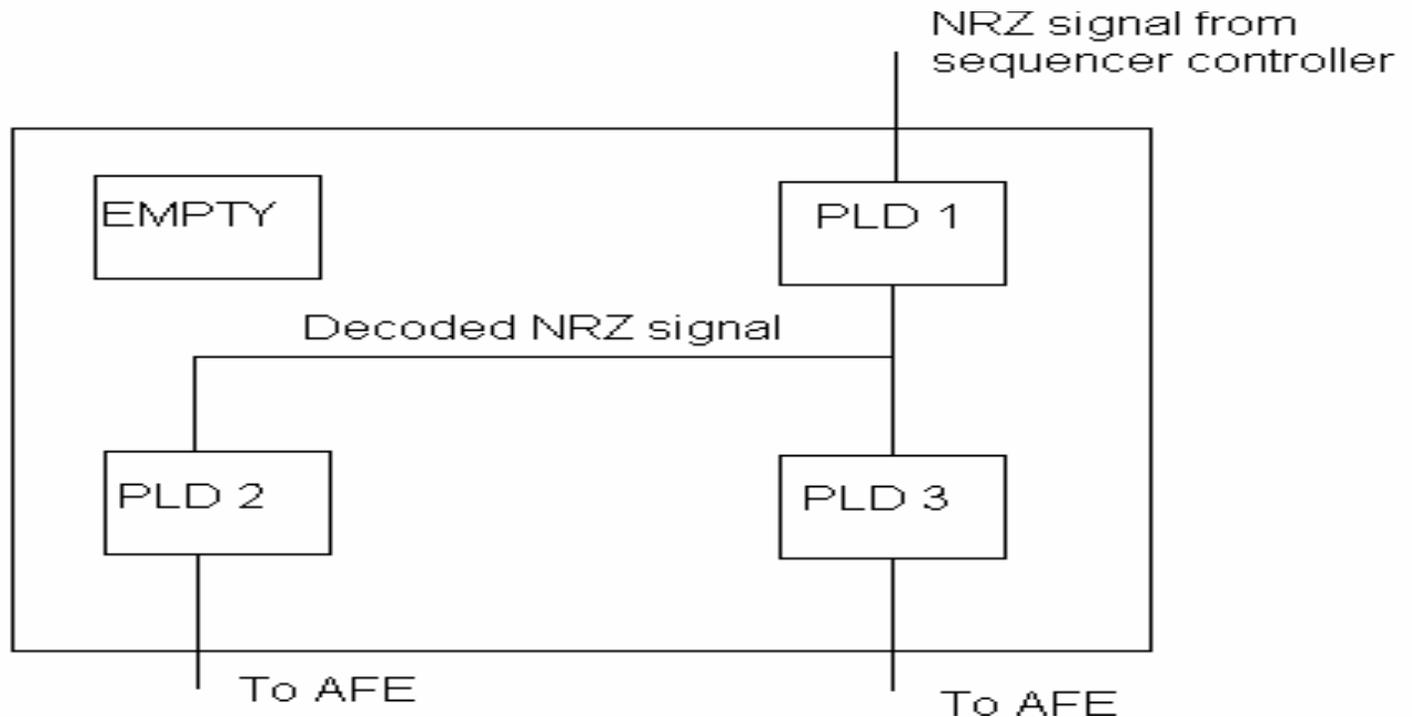


DELAY TIMES REQUIRED

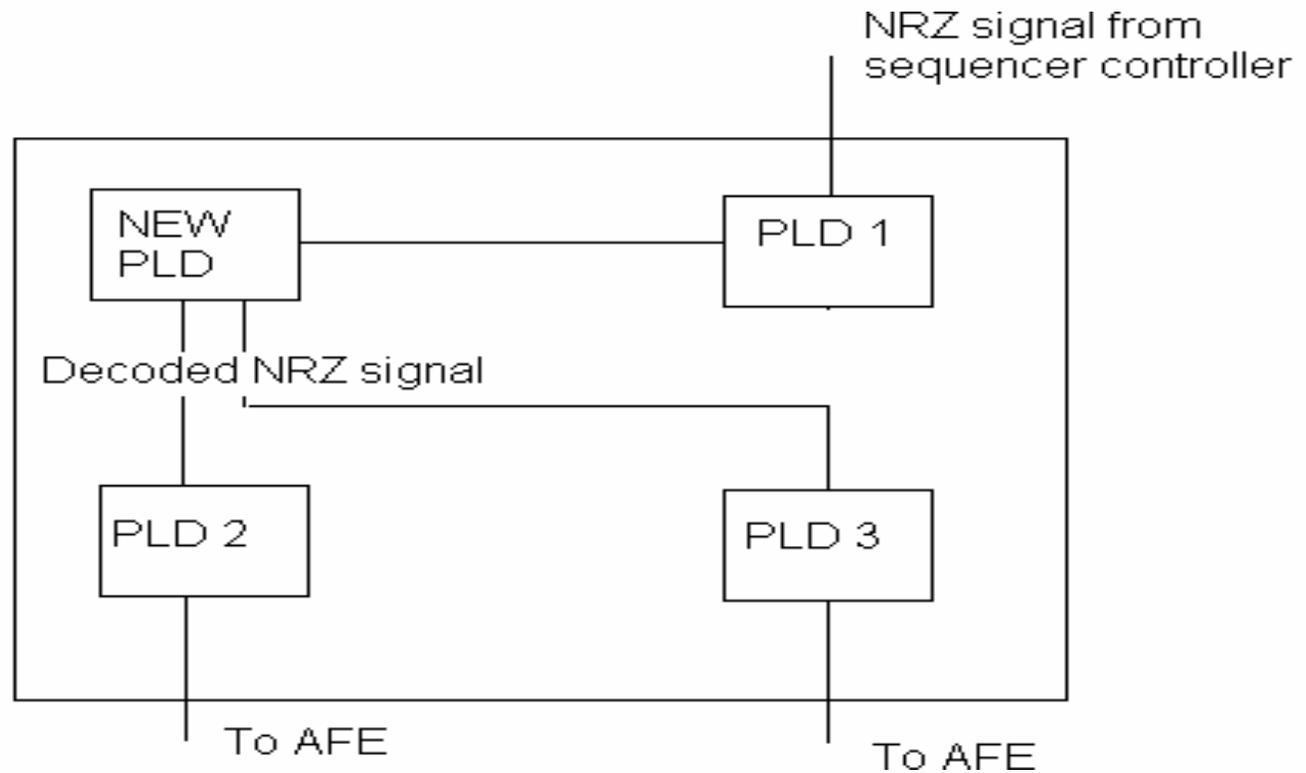
The theoretical delay times are:

- 321ns
- 575ns
- 636ns

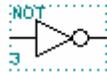
Simple block diagram of Sequencer before modification



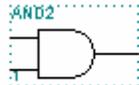
Simple block diagram of Sequencer After modification



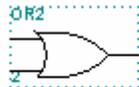
Digital Logic 101



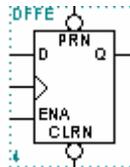
NOT



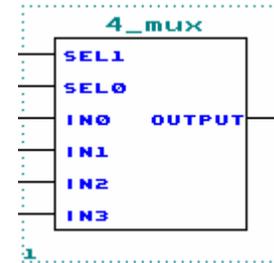
AND



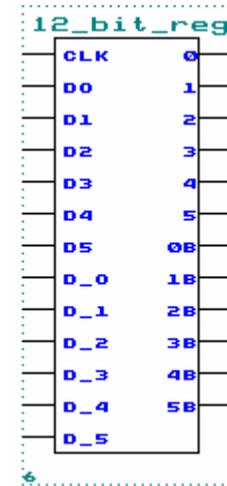
OR



D-flip-flop

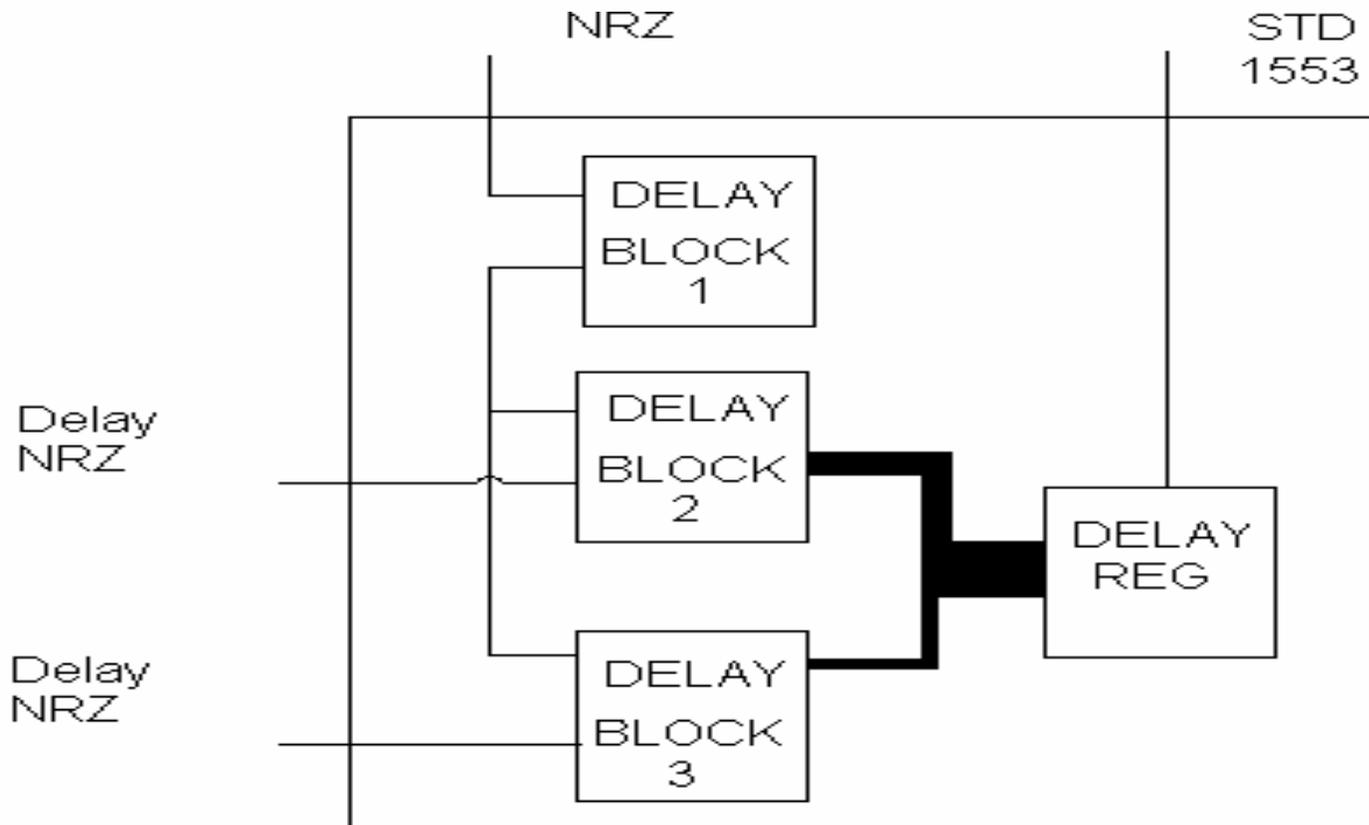


4-1 multiplex

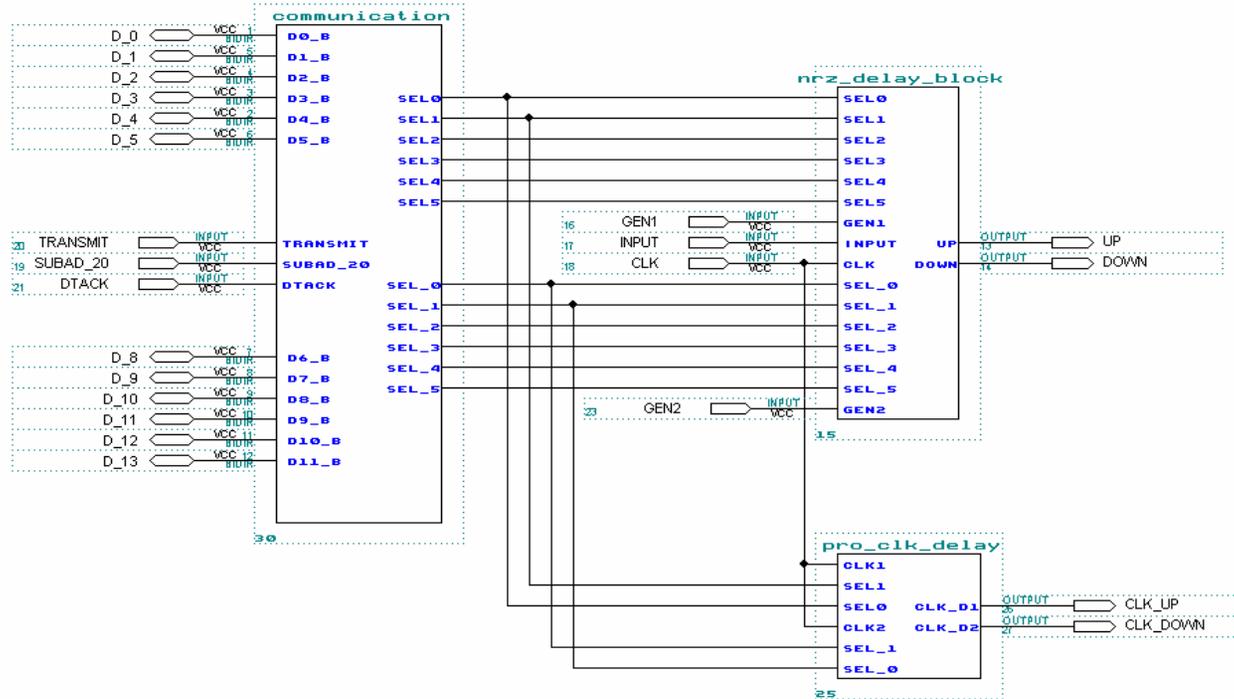


12 Bit Register

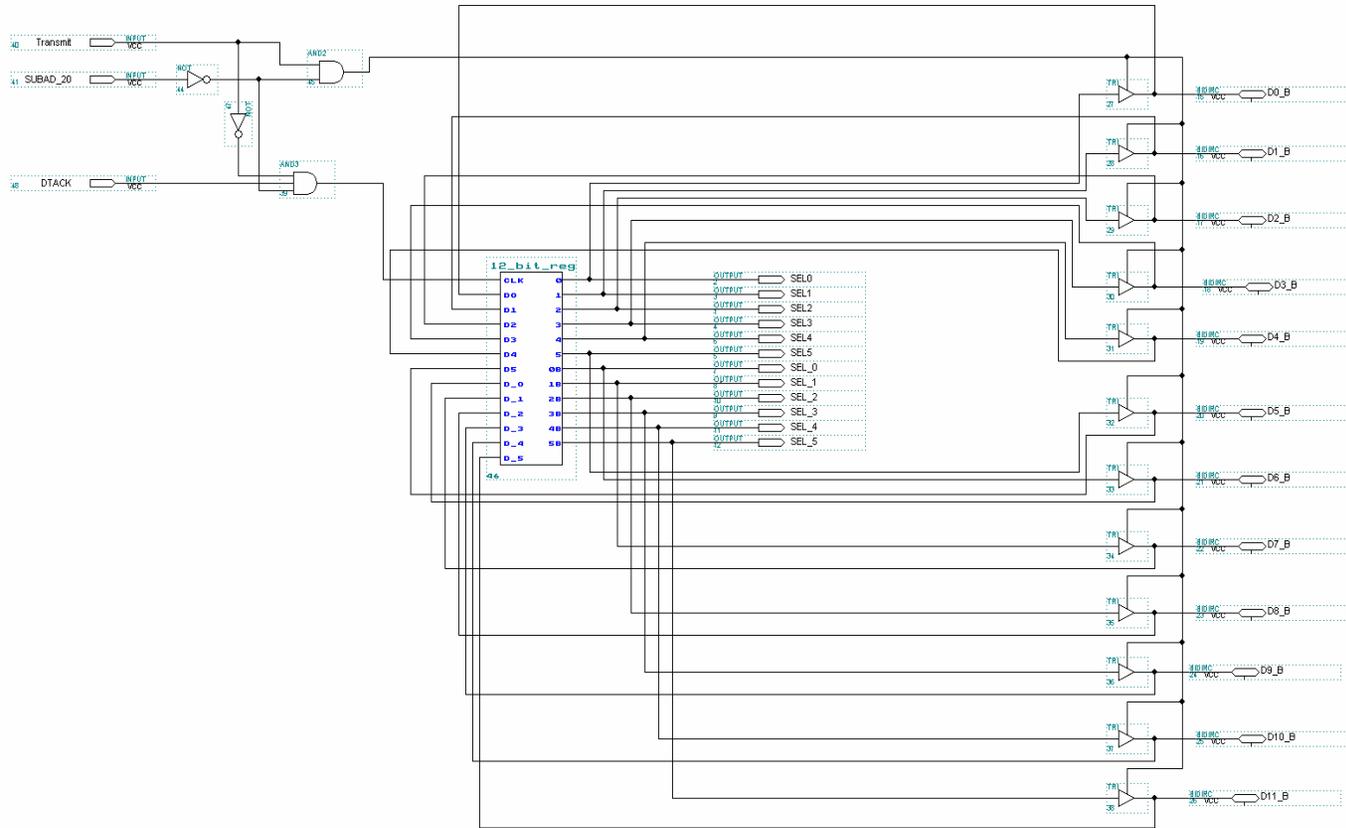
Block Diagram of the NEW PLD



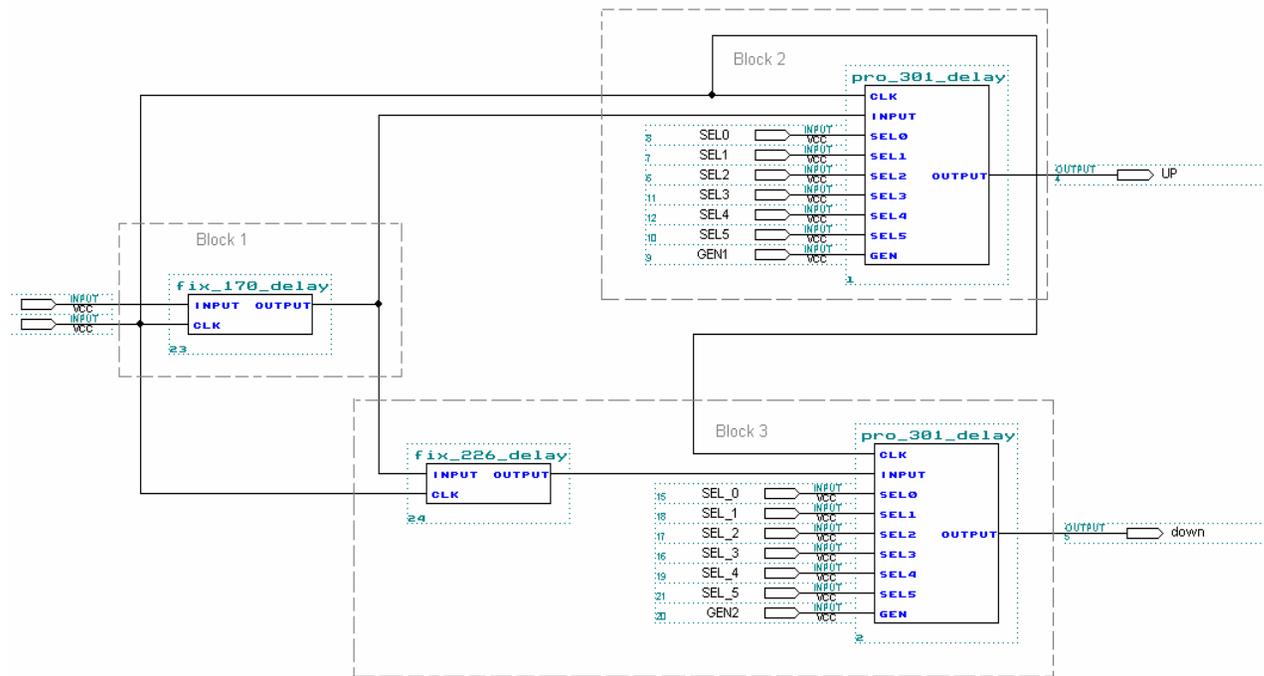
Schematic of version 1



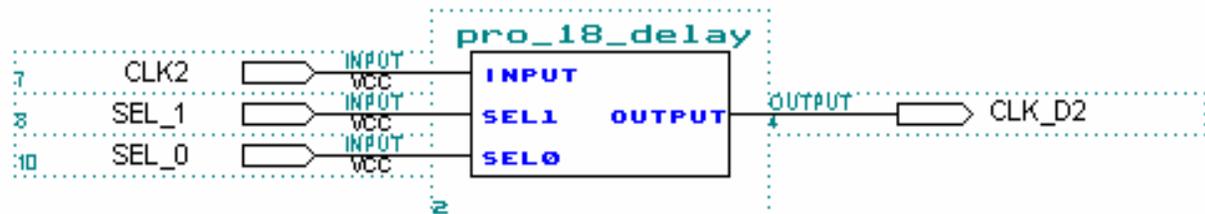
Schematic of Communication



Schematic of NRZ delay Block.



Schematic of programmable clock delay





Conclusion

How delays help the physics

- Allows the FPD data be integrated into the system

Simulation results show that

- Min delay for Upper PLD is 188.8 ns
- Max delay for Upper PLD is 414.4 ns
- Min delay for Lower PLD is 494.8 ns
- Max delay for Lower PLD is 720.4 ns
- Resolution of about 5ns