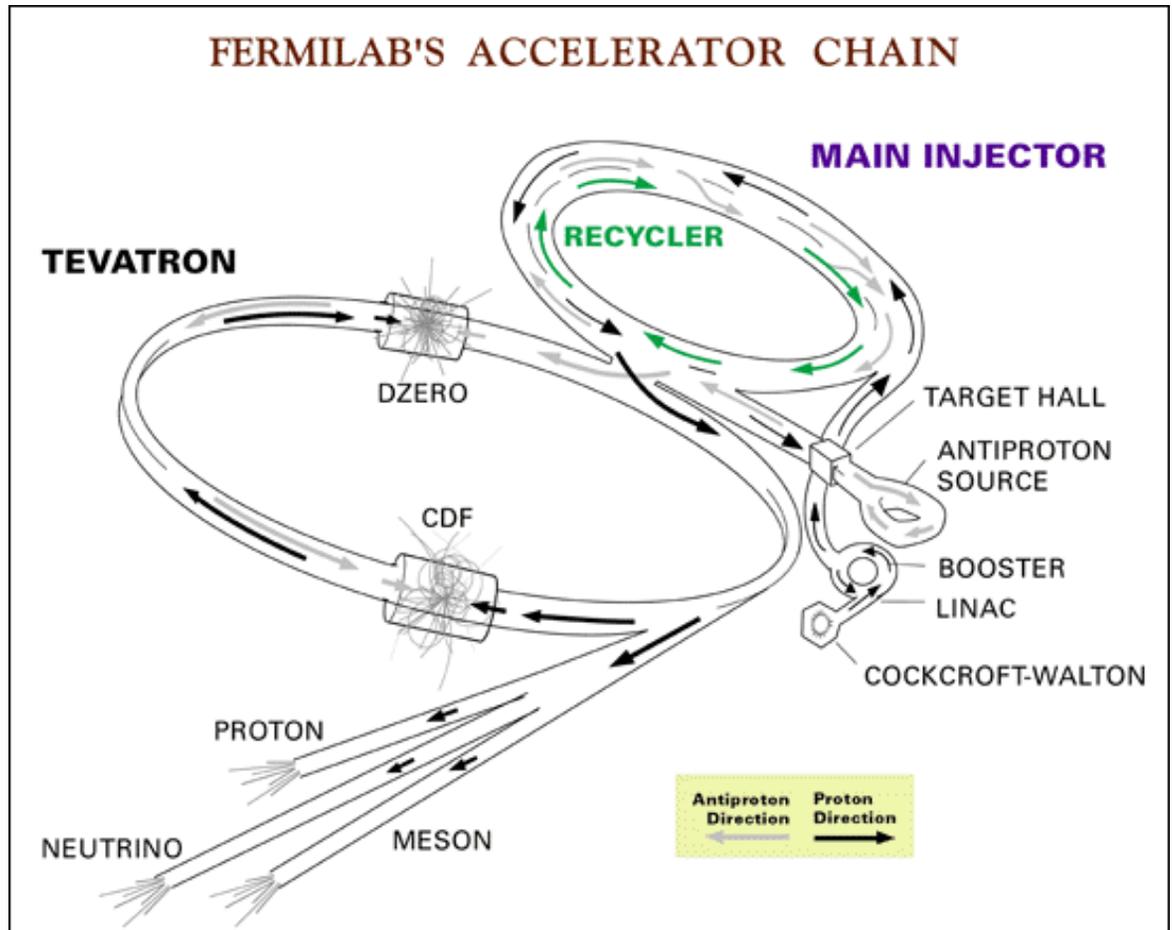


From the Very Big to the Very Small (Electrical Engineering at Fermilab)

Ray Yarema
FNAL Engineer
July 5, 2006

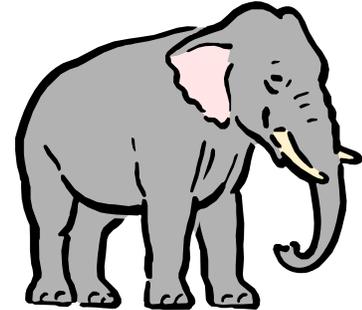
Fermilab Accelerator Laboratory

- What does electrical engineering have to do with accelerators?
- Lots!!!!



Electrical Engineering At Fermilab Covers a Broad Spectrum

- Power engineering
 - Power distribution
 - Power conversion
 - Pulsed power systems
- RF system and circuit design
- Controls for accelerator and processes
 - Liquefying Helium
- Instrumentation
 - Accelerator
 - Beamlines
- Data Acquisition
- Circuit board design
- Detector Electronics
- Integrated Circuit design (ASICs)



Big



Small

Electrical Engineering

- Electrical Engineers collaborate with others on projects
 - Mechanical engineers
 - Cryogenic engineers
 - Physicists
- Electrical engineers at Fermilab deal with state of the art problems
 - High power distribution and usage
 - Extreme temperature variations
 - High speed electronic performance
 - High reliability applications
 - Very small electrical signals
 - Extremely small mass and space requirements for circuits
 - High radiation environments for electronics

It all Starts Here

- Power is brought on to the Fermilab site at 345kV
- At the master substation the voltage is reduced and sent around the lab to power magnets in the accelerator and everything else

Master power substation



345 kilovolt power line

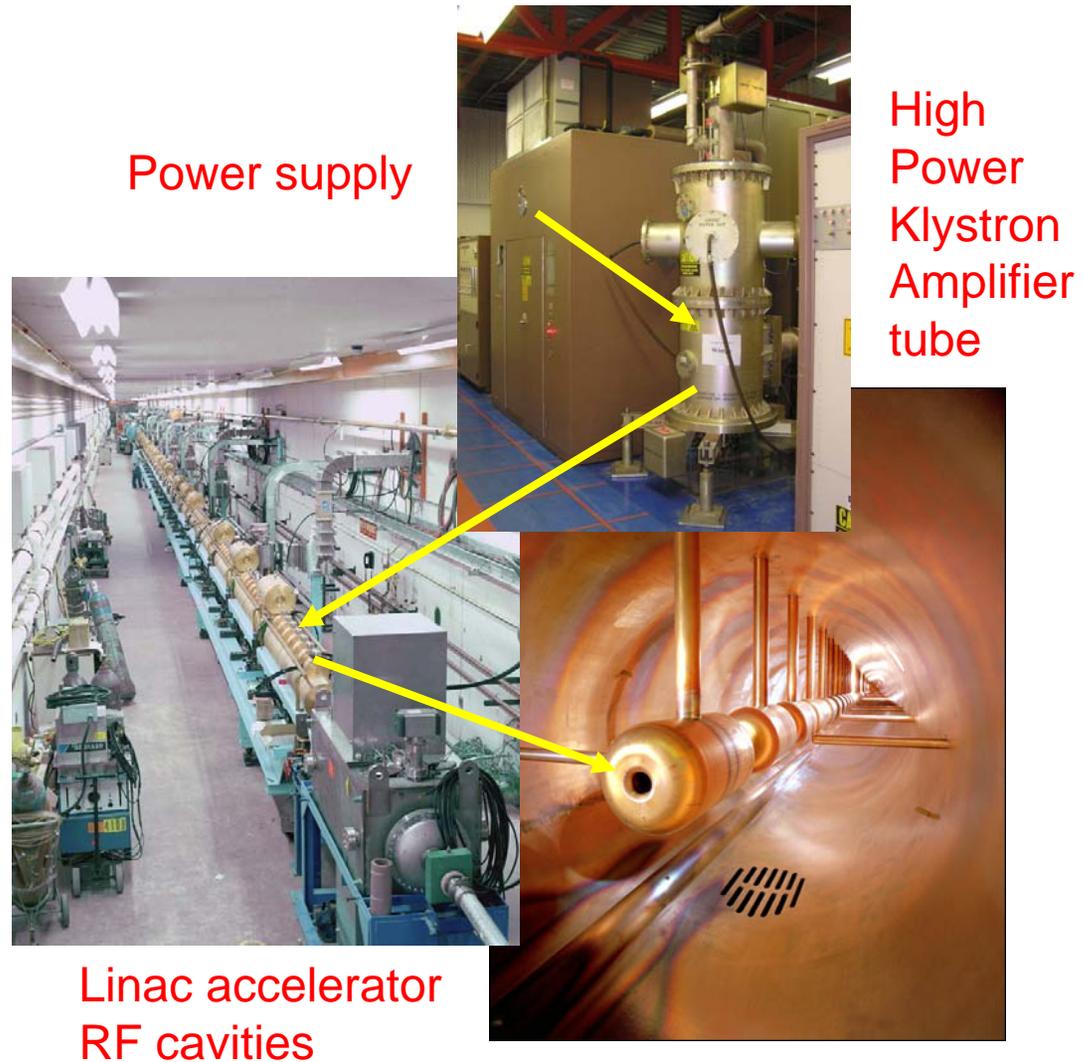
Large power supplies



Magnets for steering
And focusing beam

RF Engineering

- Radio Frequency (RF) electrical signals are used to accelerate the beam in most accelerators
- RF components can also be very large.



Many Processes Need Electronic Controls

- Liquification of helium for cryogenic magnets
- Treatment of patients at Fermilab Neutron Therapy Facility
- Controls for water, vacuum, lighting, etc

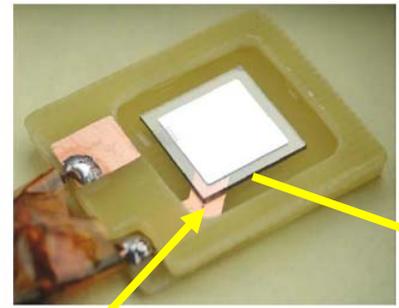
Vertical CT Scanner
At the Neutron Therapy
Facility



Central
Helium
liquifier

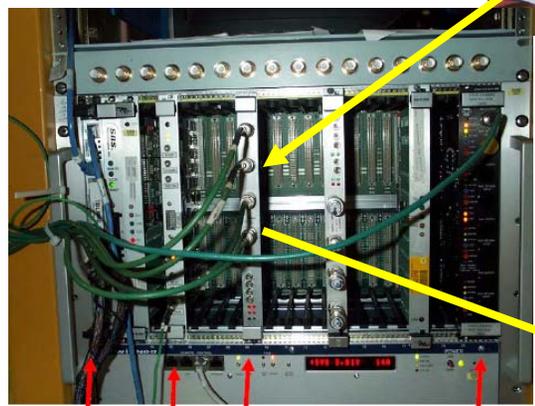
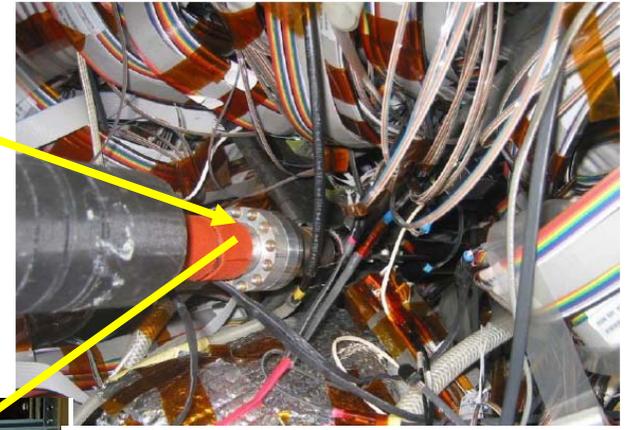
Instrumentation

- A great deal of work goes into instrumentation for accelerators and beam lines
 - Beam position monitor (BPM)
 - Beam loss monitor (BLM)
 - Beam condition monitor (BCM)
 - Uses large diamond mounted near the beam
 - Safety systems
 - Many others

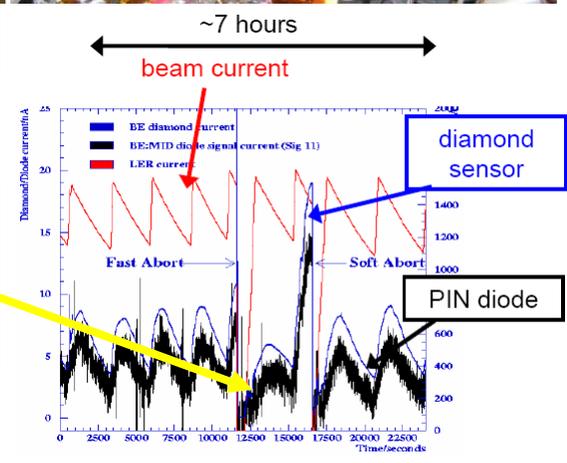


A G10 packaged diamond:
2.2cm(w) x 2.5cm(l) x 0.7mm(t)
7 grams

Sensor in inaccessible area
On detector

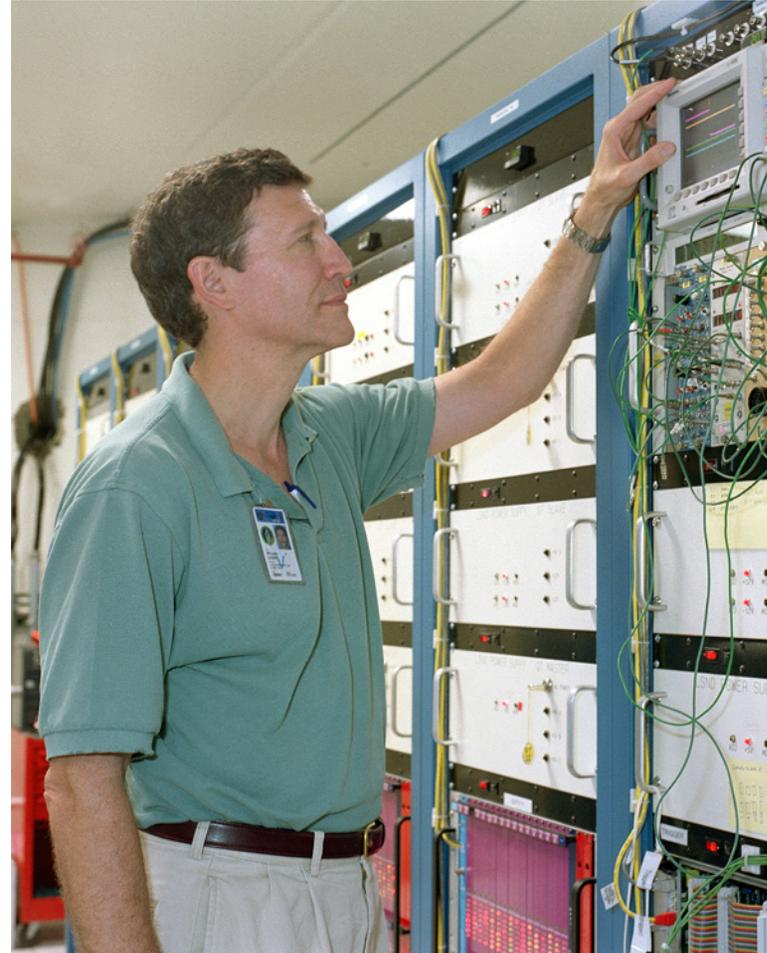


CPU Timing Digitizer High voltage



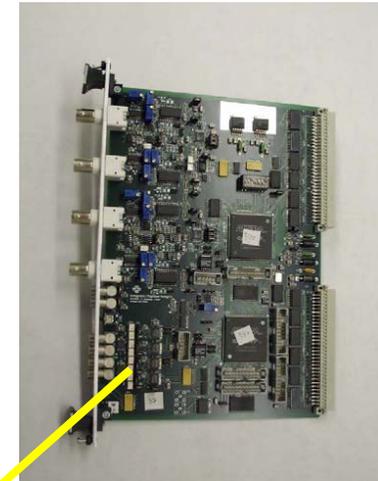
Data Acquisition

- The purpose of all experiments is to record data for analysis
- Generally done with embedded computer systems located at the experiment.
- Data is transmitted to "computer farms" for later analysis.

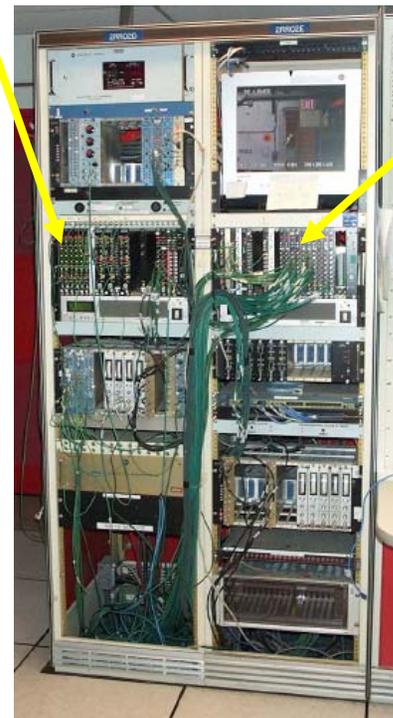


Circuit Board Design

- Many specialized circuit boards are designed at Fermilab
 - Sizes range from 1 in² to 1 m²
 - Analog and digital designs
 - Frequently use special materials
- Boards are placed in crates which are mounted in racks.
- Power, cooling, temperature sensing are usually a part of the electronic rack design



Circuit board

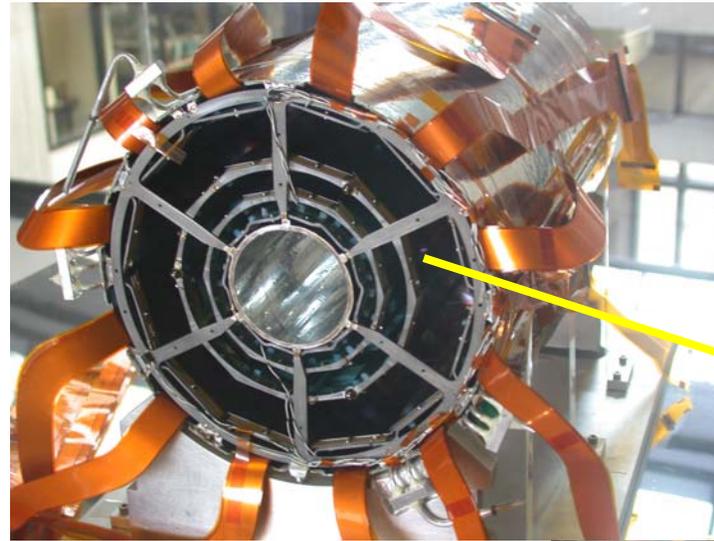


Several crates
In two racks

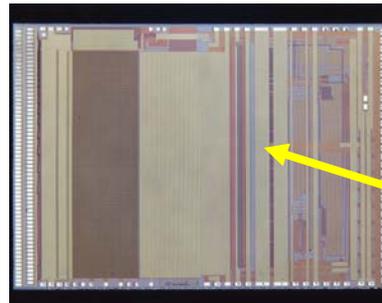
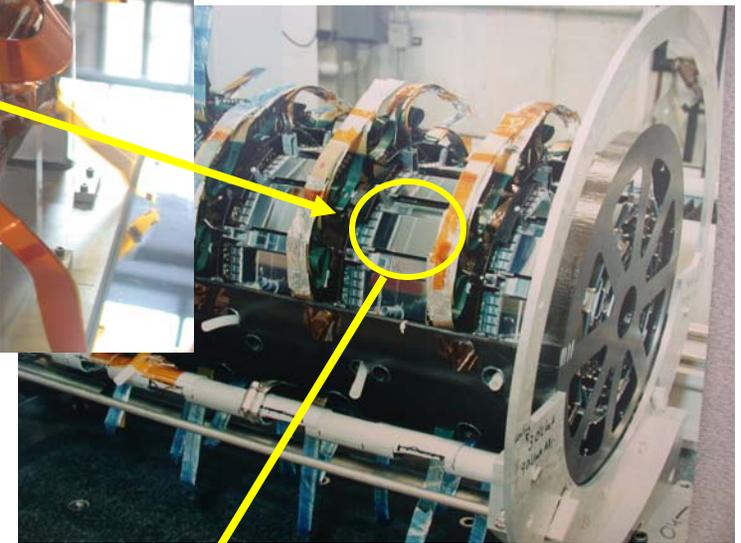
Detector Electronics

On display on WH 15N

- Large number of channels of electronics per experiment (10K to 500M)
- Requirements:
 - Low mass
 - Low power
 - High speed
 - Radiation tolerant
 - Low cost
- ASICs have become essential in detectors

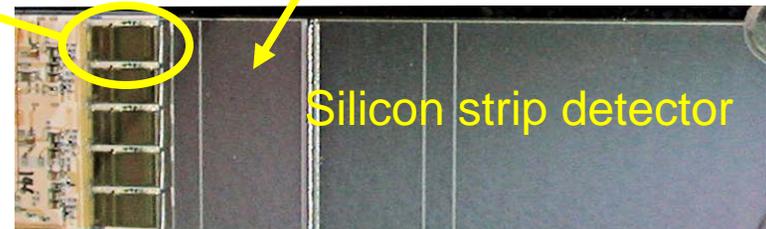


CDF silicon strip
Vertex detector –
Used to find top quark



Readout
chip

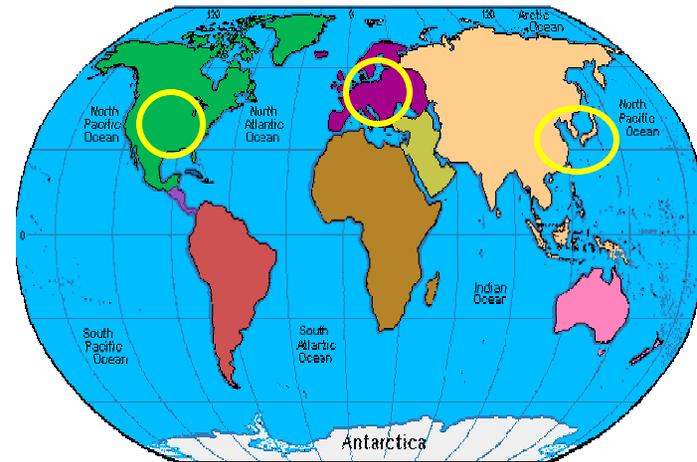
128 channel
Silicon strip readout
Chip (6.4 x10 mm)



Silicon strip detector

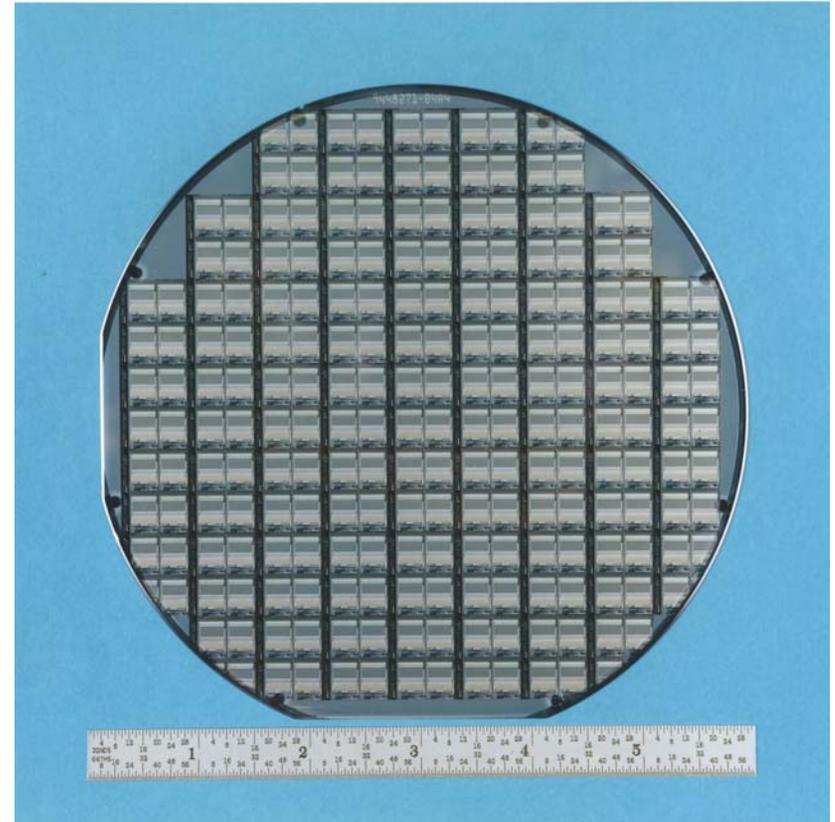
Application Specific Integrated Circuits (ASICs)

- ASICs are now found in essentially all high channel count High Energy Physics experiments.
- ASIC design requires special education and sophisticated software tools for simulation and layout.
- Design files are sent to outside foundries for fabrication.
 - Hong Kong
 - Austria
 - USA
- ASIC design at Fermilab is done in PPD/EED



ASIC Fabrication

- Up to 25 masks (similar to photographic negatives) are needed for each design.
- A set of masks now costs from \$50K to \$1 M depending on the technology used.
- It can take from 8 weeks to 6 months to get a device back from the foundry.
- ASICs are made on wafers (4 to 12 inches in diameter)
 - An 8 inch wafer may cost \$5K and have a 1000 parts on it
 - Not all parts are good (80% yield is typical)
 - Wafers are diced and parts are usually put in packages for mounting on circuit boards

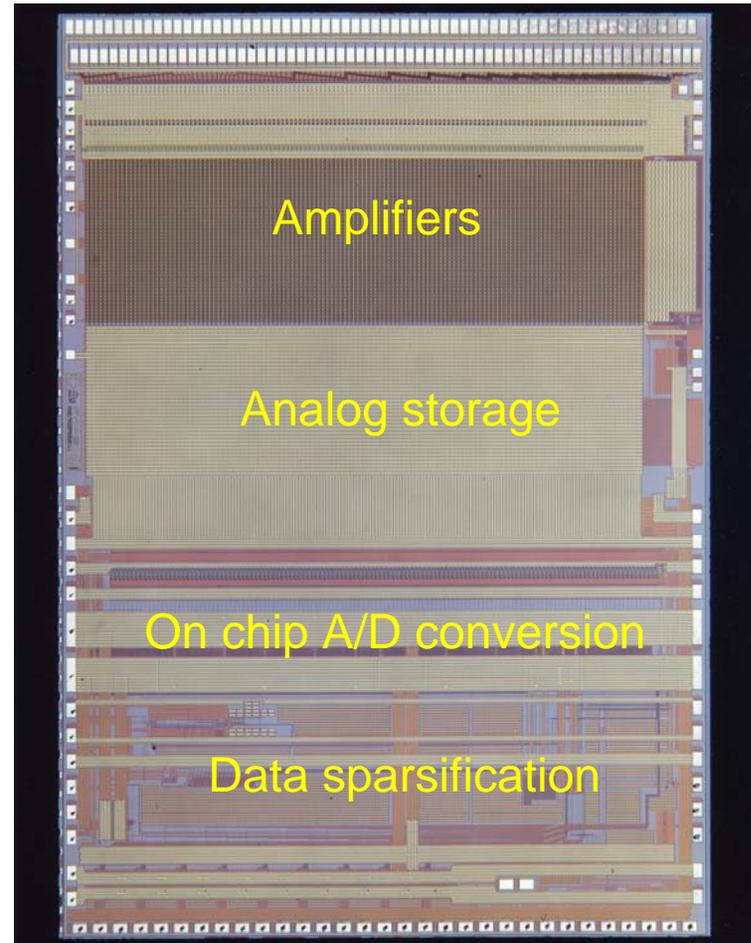


Focusing on the Very Small: Look at some ASICs

- SVX4 installed at DO also for Brookhaven
- FPIX for BTeV but now used at BNL
- QIE 8 for CMS
- APD for NOVA
- A few other Photos
- The future has us working on even smaller circuits - ILC 500 M channels of pixels

SVX4

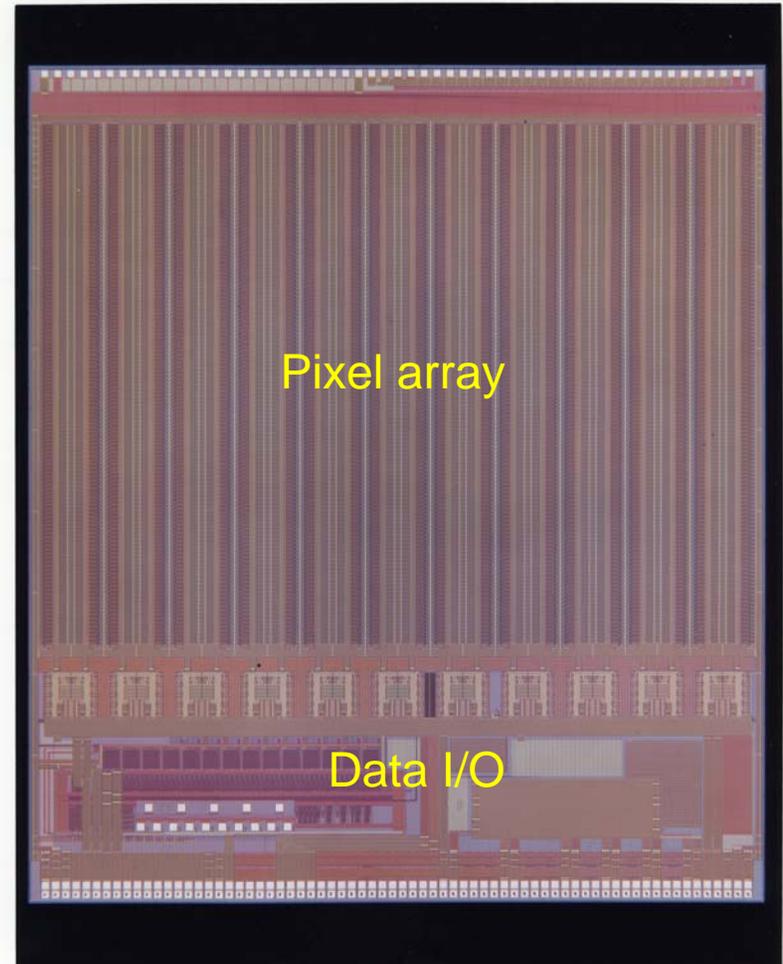
- Fourth design in a series of ASICs for the CDF and DZero experiments
- Each succeeding design has more stringent requirements
 - Speed
 - Radiation tolerance
 - Size
 - Features
- Latest design includes:
 - 128 channels
 - Continuous data read and write
 - Low noise amplifiers
 - Analog storage
 - On chip A/D conversion
 - Data sparsification
 - Deep submicron feature sizes
 - Radiation tolerance of 50 Mrads (by design)
 - Wire bonds to detector
- Just installed in layer Zero at DZero - also to be used at BNL.



6.3 x 9.0 mm, TSMC 0.25 μ CMOS

FPIX2 (Fermilab Pixel 2)

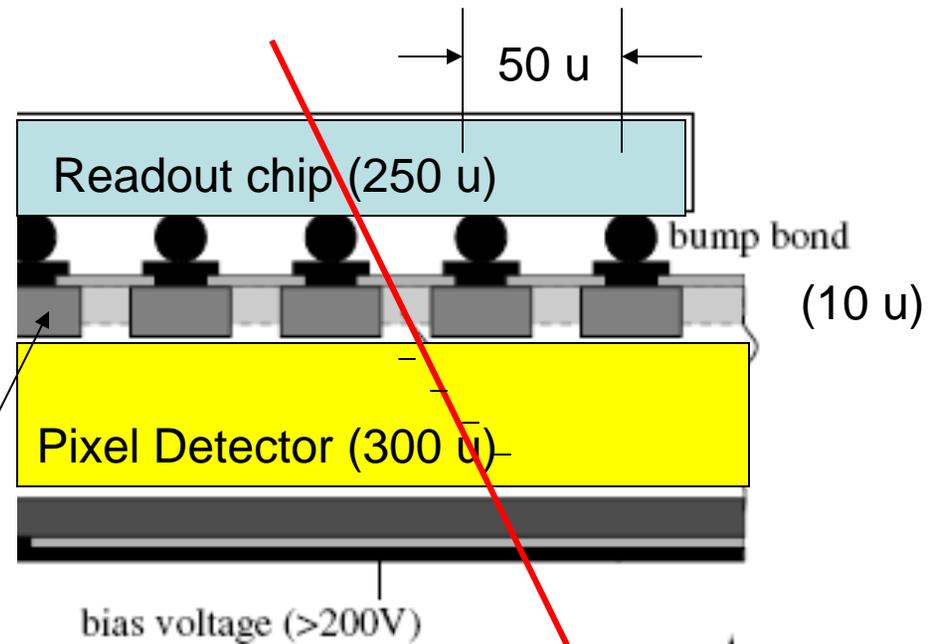
- Pixel sensor chips are used to track particles and provide very fine resolution
- Readout chip for pixels, designed for BTeV experiment
- Will be used in Phenix experiment at BNL
- Chip has 128 rows by 22 columns, 2816 pixels/chip
- Each pixel
 - 50 x 400 microns
 - Includes 3 bit ADC
 - High speed, 840 Mbit/sec readout
 - Data used in level 1 trigger
- Chip is radiation hard by design
- Chip is bump bonded to sensor



8.9 x 10.1 x 0.3mm,
TSMC 0.25 μ CMOS

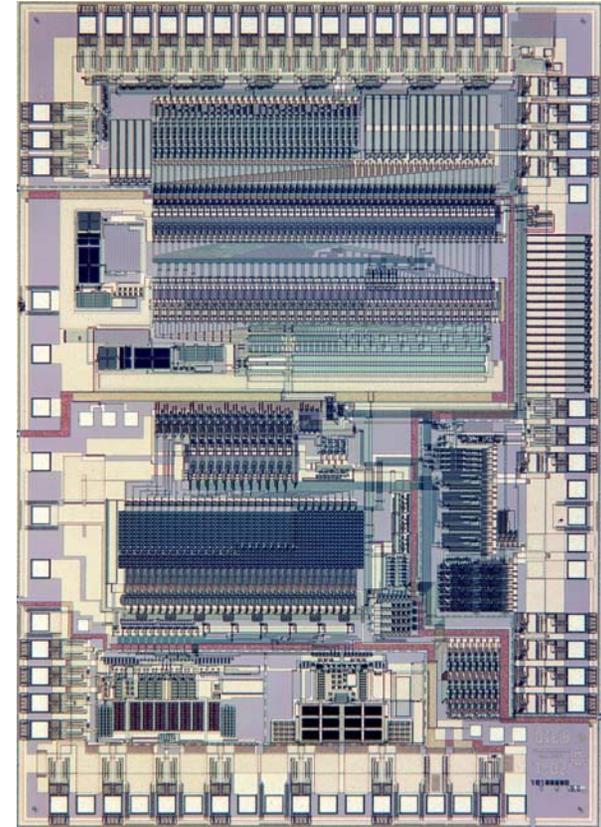
Pixel detector and Readout Chip Assembly

- A pixel readout chip is bonded to a pixel sensor chip using small solder bumps
- Particles pass through both the readout chip and the pixel array
 - The sensitive area in the readout chip is very small
 - The detector has a much larger sensitive volume where charge is generated.
 - Charge is collected on the pixel electrode where it is transmitted via the bump bond to the pixel readout chip where it is amplified and readout.



Photomultiplier Tube Signal Processor with Auto Ranging ADC

- QIE 8 was designed for the Compact Muon Solenoid experiment at CERN
- Takes wide dynamic range signal from a PMT, splits the signal into weighted parallel paths, selects the appropriate path, digitizes the signal and outputs a value in a floating point format.
- Connections made with 25 μ wire.
- To be installed next year.



3.0 x 4.3 mm, AMS 0.8 μ BiCMOS

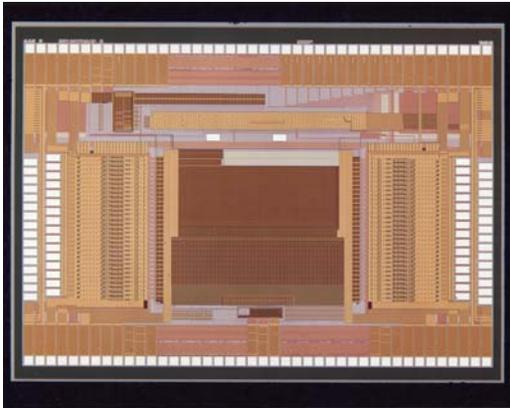
Avalanche Photo Diode Readout Chip

- APD readout chip designed for NOVA experiment which is to be built in Minnesota
- Used to look at neutrinos from Fermilab or neutrinos from outer space.
- Chip features
 - 32 channels for compact design
 - Low noise (150 e) because of the very small signals obtained from APDs
 - Many programming features to allow the chip to operate in different modes with different gain and speed.
 - On chip 10 bit ADC
 - On chip 64 stage analog pipeline

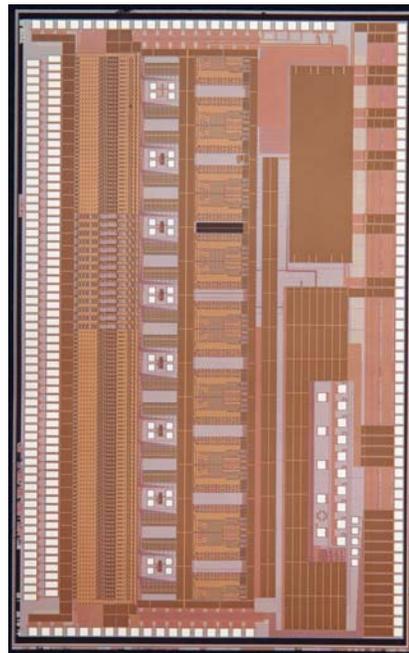


2.6 x 5.6 mm,
TSMC 0.25 μ CMOS

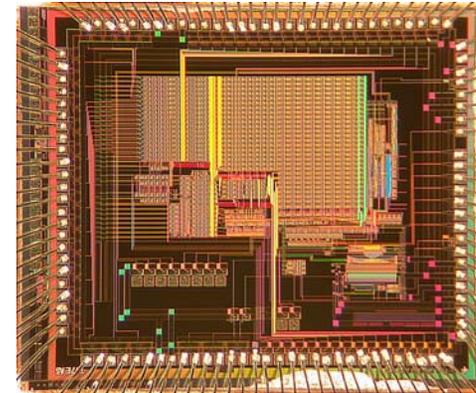
Many Different Chips for Many Different Experiments/projects



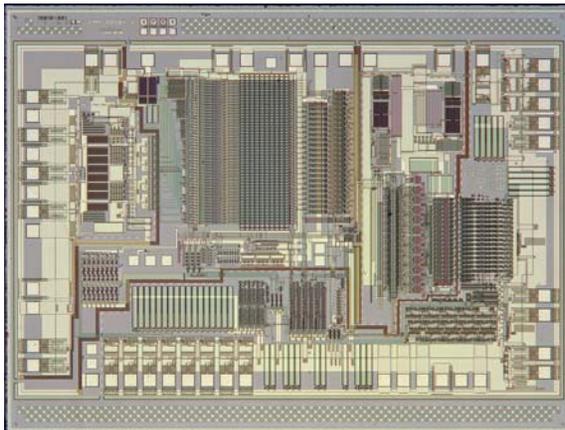
DCAL for ILC



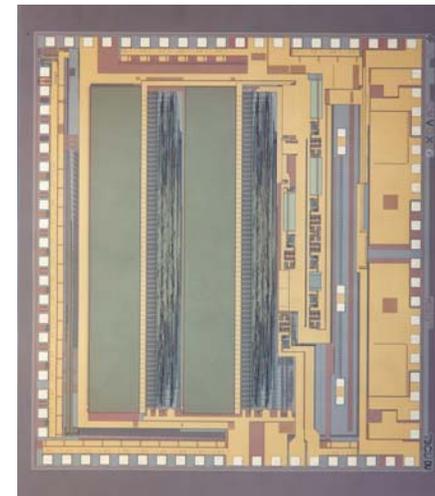
FSSR for BTeV



CCA for CMS



QIE 9 for BTeV



RMCC for PMTs

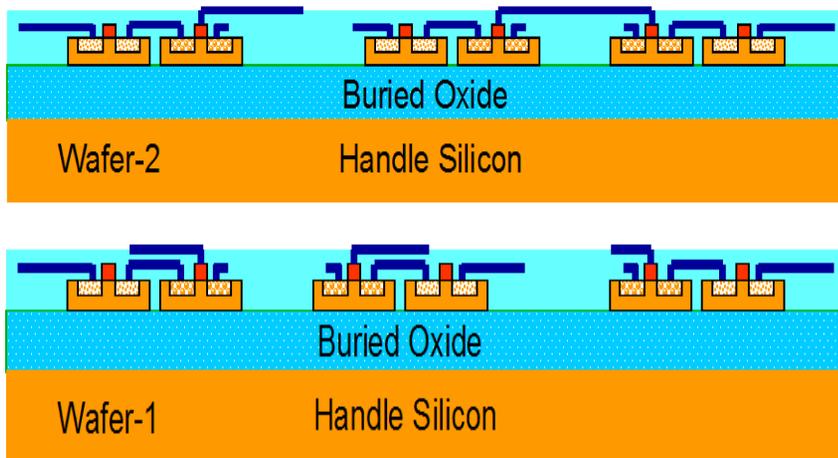
Latest Fermilab ASIC R&D Initiative

- Nearly mass less circuits are needed for some new experiments like the ILC
- Fabricate electronic circuits on very thin substrates, less than 10 microns thick (1/5 the thickness of a human hair).
- Bond the substrates together
- Make 60 million 1 micron diameter interconnects between the chips on the wafers.
- Goal - Make 500 million channels fit inside a small coffee can size enclosure and dissipate very little power.

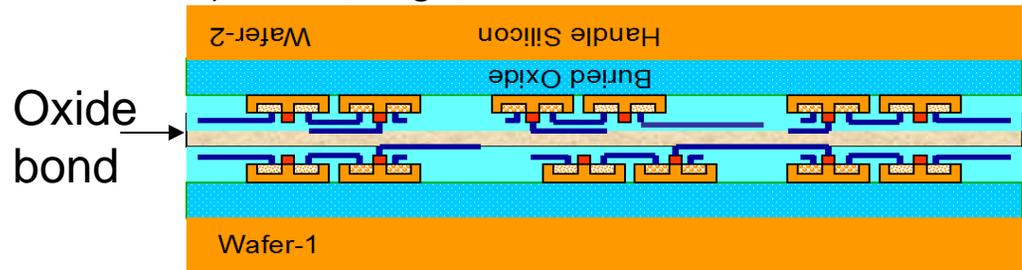
Multilayer (3D) ASICs

- 3 tier chip 0.18 microns (all layers)
 - SOI process simplifies via formation
 - Thin each layer 1/5 thickness of human hair
- 2×10^9 Transistors/layer, 60×10^6 vias/layer, 1 μ metal filled vias

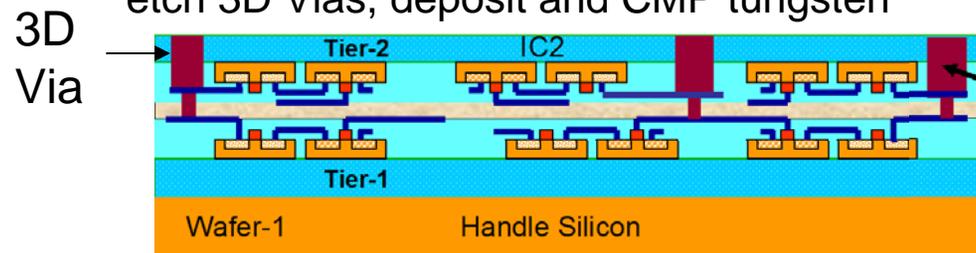
1) Fabricate individual tiers



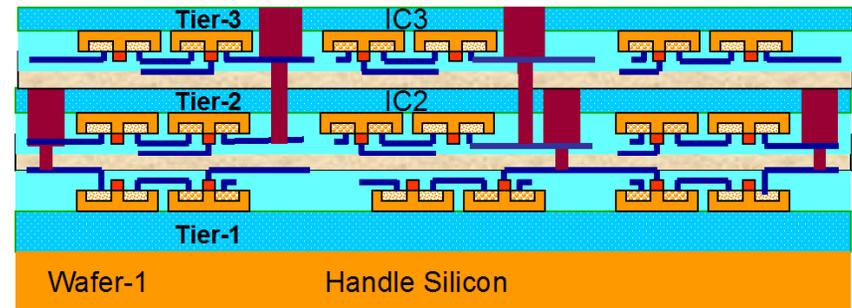
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1, remove wafer 3 handle wafer, form 3D Vias from wafer 3 to wafer 2



Summary

- There are many aspects to electrical engineering at Fermilab.
- Each one offers its own set of opportunities and challenges.
- Big scale projects deal in megawatts while small scale projects deal in microwatts.
- From the very big to the very small, Fermilab electrical engineers do it all!!